Electrical properties of Cadmium Telluride Thin Film Solar Cells Activated with Magnesium Chloride

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This thesis is dedicated to the memory of Professor Murat Bayhan,
a cherished scientist, teacher, and friend.

Abstract

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This thesis presents a systematic study into the effects of device processing on electrical parameters for cadmium telluride solar cells. In order for high efficiencies to be achieved, it is essential to treat CdTe solar cells with chlorides in a post-growth process. For the past 30 years the treatment of choice has been with $CdCl_2$, although it is expensive and is known to be toxic. Recently alternative chlorides have been investigated and it has been demonstrated that cells produced using $MgCl_2$ have efficiencies comparable to the best made using $CdCl_2$. $MgCl_2$ is both cheap and non-toxic. Deep and shallow traps were studied with capacitance voltage ($C-V$) analysis and thermal admittance spectroscopy (TAS). Current density-voltage-temperature ($J-V-T$) measurements were used to determine the transport mechanisms of as-deposited and processed devices. Equivalent circuit models were explored using frequency response analysis (FRA) data. A study of the deep traps was performed using thermal admittance spectroscopy (TAS). It was found that $MgCl_2$ activates CdTe devices in a similar manner to $CdCl_2$, with electrical parameters similar to those reported in literature for $CdCl_2$. Devices demonstrated a continuously varying deep trap with the degree of $MgCl_2$ processing, with the shallowest traps ($\sim 0.22\,\mathrm{eV}$) in the most efficient devices (reduced from $\sim 0.40\,\mathrm{eV}$ in under-treated cells). This is consistent with the Shockley-Read-Hall recombination process. A peak in shallow doping also was found in optimised devices with uncompensated acceptor density measured to be $\sim 3 \times 10^{14}\,\mathrm{cm}^{-3}$, an order of magnitude larger than in untreated devices.

The effects of thermal annealing alone were compared to annealing in the presence of $MgCl_2$. It was found that chloride processing improved device response more than annealing alone, with a corresponding improvement in electrical parameters. Combining the treatments, with a thermal anneal followed by chloride processing, demonstrated further performance enhancement. The window layer used in the devices was found to affect the efficiency and electrical parameters, with CdS:O CdTe producing higher efficiency solar cells than CdS/CdTe.

The impact of doping at the back contact was investigated through additional layers of copper or copper thiocyanate. Although both improved device efficiency, copper thiocyanate increased shallow doping more with consistent observation of traps thought to be related to copper defects.

Declaration

I declare that with the exception of those procedures listed below all the work presented in this thesis was carried out by the candidate. I also declare that none of this work has been previously submitted for any degree and that it is not being submitted for any other degree.

Sample sets and devices in this work were designed and manufactured by members of the working group at the Stephenson Institute for Renewable Energy:

- Dr. J. Major (Series 521, 522 and 721)
- Dr. M. Al Turkestani (Series 621 and 622) (Assistant Professor at the Department of Physics, Umm Al-Qura University, Mecca, KSA)
- Dr. L. Phillips (Series 722)

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Prof. Ken Durose (Supervisor)	Dr. Annette Pressman (Candidate)

The candidate was based at the University of Liverpool for the period of October 2013 - September 2017.

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Contents

T H E S I S

1. Introduction

1.1 Context

Energy requirements continue to grow with a predicted yearly increase of 1.3 % up to 2030 [1]. Currently, solar power generation accounts for <1% of the global supply [2]. There is a colossal amount of solar power that is as yet untapped; if an area the size of the USA were covered in solar modules, the yearly global requirement would be met in under two minutes (see Appendix D). The photovoltaic market is dominated by silicon. Multi-crystalline panels are the market leader, followed by mono-crystalline. However, cadmium telluride (CdTe) is the leading thin film technology and accounts for 4% of the market share. CdTe modules have similar efficiency to the market leader, and at \$0.53 /Wp (Watts at peak power) are also cheaper (according to the US manufacturing cost estimates 2013) [3–5]. Although the module efficiencies of mono-crystalline silicon are still significantly higher that the thin-film technology of CdTe (figure 1.1 b), the reduced cost for CdTe modules is significant.

Cadmium telluride has several physical advantages over silicon. The high optical absorption of CdTe allows a 1 µm CdTe film to absorb the same 92% of light that a 200 µm layer of crystalline Si would do [6]. This allows for thinner films of CdTe, and the poly-crystalline nature of CdTe thin films allows for easier manufacture. CdTe is a direct band gap material and higher temperature dependent performance than silicon [7]. With a band gap of $E_g = 1.45\,\text{eV}$ CdTe it is able to extract close to the maximal possible energy from insolation according to the Shockley Quiessar limit [8, 9], which is not the case for silicon.

There are emerging technologies and concepts in photovoltaics in areas such as hybrid perovskites, organic PV and the use of materials with sustainable feedstocks, but there is still a research and development investment required to bring these to market. For long-term prospects, sources of tellurium are not guaranteed to satisfy the demand as it is commonly a by-product of copper mining. Some have concerns about the environmental impact of recycling CdTe modules.

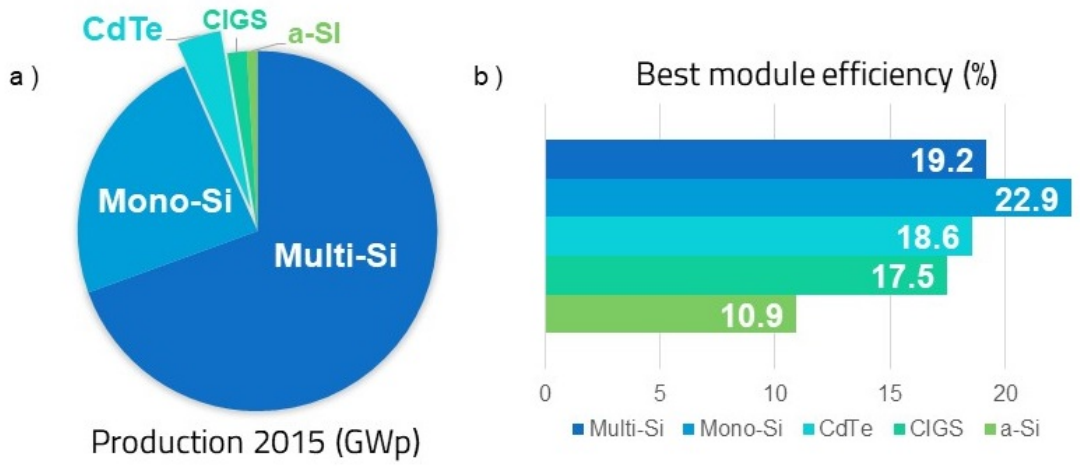

Figure 1.1: Charts to demonstrate a) the market split between different photovoltaic modules in 2015, and b) their average module efficiency [10]. The materials are multi-crystalline silicon (multi-Si), mono-crystalline silicon (mono-Si), and the thin film technologies; cadmium telluride (CdTe), copper indium gallium sulphide (CIGS) and amorphous silicon (a-Si).

Nevertheless, the medium term use of CdTe would allow the saturation of the photovoltaic market until new technologies become economically viable. However, despite the position of CdTe in the marketplace and the 40 year history of research into this complex material, it is believed there are still further improvements that can be made which would enhance the efficiency of PV devices.

1.2 Motivation

The subject of this thesis is the study of the electrical properties of cadmium telluride solar cells: it is an investigation into how materials processing, material layers and even electrical contacts affect parameters that control the device performance. For the early years of CdTe development, so-called 'type conversion' from n- to p-type was conducted by post-growth annealing to produce record performance device efficiencies $> 10\%$ [11, 12]. This step is critical to obtain working solar cells. Attempts to treat thin film device with $CdCl_2$ after deposition resulted in continued enhancements in performance [13]. The current record laboratory efficiency stands at 22.1% for a polycrystalline device (First Solar, 2016 [14]). Despite 40 years of research, this value falls somewhat short of the theoretical maximum of $\sim 29\%$ [15, 16]. The shortfall is primarily in the voltage achieved, since the currents collected are close to the theoretical limit [17]. Mono-crystalline CdTe devices have recently broken the 1 V barrier for the open circuit voltage (V_{OC}), but for polycrystalline cells the record is ~ 0.9 V [18–20]. The parameters

affecting V_{OC} are therefore of great interest, as once understood and controlled there is the scope for this complex material to produce an extremely efficient and cheap energy source. As such there have been many studies made of $CdCl_2$ treated devices [21–24].

In recent years it has been demonstrated that the toxic $CdCl_2$ processing step can be replaced by the use of other chlorides [25, 26]. In particular, treatment with magnesium chloride has produced cells of similar efficiency and behaviour to $CdCl_2$, and it has substantial advantages: it is very cheap, easy to use, and is demonstrably non-toxic (it is used in the food industry to coagulate tofu under the name 'nigari'). It has the potential to reduce the costs and environmental impact of CdTe photovoltaics. All of the chloride processed devices studied in this work use $MgCl_2$, or annealing, or a combination of the two to create working devices. Systematic studies are reported here on the behaviour of device working parameters alongside more fundamental materials characteristics, particularly deep levels (i.e. 'trapping' levels that compromise V_{OC} and contacts), and shallow levels that facilitate doping. The techniques used involve electrical characterisation under DC and AC conditions, measuring variable such as current, capacitance and impedance as functions of frequency and temperature.

The layers of a CdTe device are shown schematically in figure 1.2. As it is possible to attain higher V_{OC} in single crystal devices, it is likely that interfaces are a significant cause of voltage loss. This work is confined to the study of three compositional layers in particular:

Metal back contact Gold is used in figure 1.2 and in all the devices in this study. However it is not an ideal material, as an Ohmic junction is not possible between CdTe and Au. This is explored in chapter 7.

***p*-CdTe** This is the absorber layer where incident light is absorbed and generates charge carriers. Without processing with a chloride salt or annealing the photo-activity of this layer is minimal, thought to be related to loss of photogenerated carriers to destructive recombination. The effects of $MgCl_2$ on deep and shallow levels are explored in chapter 5, and annealing in chapter 6.

CdS window layer CdS is the *n*-type heterogeneous partner to CdTe. There is however a lattice mismatch between the two. Alternative window layers such as CdS:O have higher band gaps and transparency and can improve PV performance. The window layer also has the potential to affect overlying layers with issues such as interdiffusion, crystallinity and dangling bonds. The effects of the window layer on performance are studied in chapters 5 and 6.

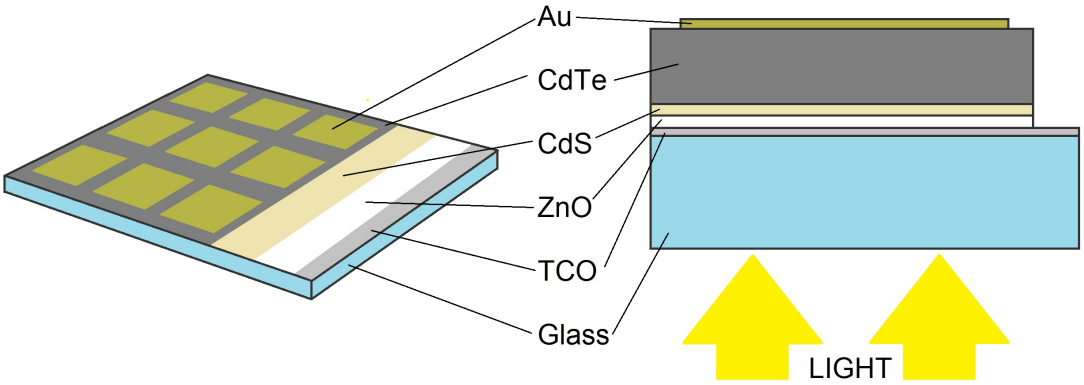

Figure 1.2: A schematic of a typical CdS/CdTe device in the superstrate configuration, grown on a glass substrate, with a transparent conducting oxide (TCO) as the front contact, optional zinc oxide layer (ZnO) ('high resistance transparent' [HRT] layer), *n*-type cadmium sulphide (CdS) layer, *p*-type cadmium telluride (CdTe) layer, and gold (Au) back contact.

1.3 Thesis structure

The structure of this thesis is as follows;

Chapter 2: An overview of the relevant semiconductor concepts, and a detailed review of issues affecting CdTe.

Chapter 3: The principles for the experimental characterisation techniques utilised.

Chapter 4: The experimental conditions for device manufacture and characterisation.

Chapter 5: A study of the relationship between the duration of chloride processing and electrical parameters (see table 1.1). The two sample sets studied here vary the window layer, with one manufactured with oxygenated cadmium sulphide, CdS:O, and the other with CdS. Both sets were then processed with $MgCl_2$ for a range of times. The resulting devices were found to demonstrate continuously variable deep trap levels.

Chapter 6: Attempts to separate the effects of thermal annealing from annealing in the presence of chlorides (see table 1.1). The first of the sample sets in this chapter compares as-grown devices with thermally annealed and chloride treated cells. Window layers of CdS and CdS:O were compared. The results were analysed with a particular focus on carrier transport. The second half of the chapter is a study comparing chloride treated samples which were given an air anneal prior to chloride treatment with identical 'control' samples which had the thermal anneal only. The air anneal was conducted at a variety of temperatures for a range of times.

Cell series	Section	Description of samples	Experimental intention
521/8	5.2.1	CdTe cells having absorber treated with $MgCl_2$ for variable times (CdS window)	Establish the effects of time dependent $MgCl_2$ treatment
522/12	5.2.2	As Series 521 with CdS:O window layer	Establish any secondary effect on $MgCl_2$ treatment from the window layer
621/6	6.2.1	CdTe samples with either a CdS or CdS:O window layer undergoing post-growth annealing or chloride treatment	Separate the effects of annealing from the chloride application (which is normally undertaken with a concomitant anneal)
622/34	6.2.2	CdS/CdTe devices annealed at different times and temperatures prior to chloride treatment	Establish if the chloride treatment and anneal effects are cumulative
721/4	7.2.1	CdS/CdTe samples with a layer of copper at the back contact	Determine the change in device characteristics with intentional Cu doping
722/4	7.2.2	CdS/CdTe cells manufactured with a layer of copper thiocyanate (CuSCN) at the back contact	Investigate the effects of a Cu-contianing layer upon performance and parameters

Table 1.1: Cell series studied in this work with their reference number/number of sample slides, where they are discussed, a brief description of the samples and the rationale behind the studies.

Chapter 7: Variations in the contact layer and their effect on cell performance were investigated (see table 1.1). The two studies in this chapter explore the effects of copper and copper thiocyanate on the underlying electical parameters of the cells that affect their performance.

Chapter 8: A discussion of the viability of the collected data and observed behaviours. The systematic errors observed throughout the thesis are considered to assess the validity of the collected data. The potential explanations behind observed trends are explored with reference to available literature.

Chapter 9: The conclusions of the thesis and potential for future work.

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2. The CdTe thin film solar cell

2.1 Solar cell operation and working parameters

2.1.1 Introduction

PV devices are based on the interaction of light with a semiconductor $p-n$ junction. The underlying physics of $p-n$ junctions is well known and outlined in many texts, see for example 'Physics of semiconductor devices' by Sze [1]. This thesis assumes knowledge of semiconductor doping, depletion region, diode behaviour of $p-n$ junctions including forward and reverse bias behaviour. Further concepts are developed as required in the thesis.

In this section PV device parameters are defined and discussed (with examples from CdTe solar cells) while the following sections provide an overview of CdTe solar cells in particular.

2.1.2 Cell characterisation

The most basic electrical characterisation of a PV device is in the form of a current density-voltage ($J-V$) relationship. From a $J-V$ plot under standard illumination, four key parameters can be extracted, and used to describe the performance of a cell. These are the open-circuit voltage, V_{OC}, the short-circuit current density, J_{SC}, the fill factor, FF and the efficiency, η. These are described below.

a) V_{OC}

The open-circuit voltage is the electrical potential across the terminals of the cell without any external load connected (see figure 2.1). It corresponds to the maximum voltage available from a solar cell. While V_{OC} arises from the band

gaps and alignment of the p- and n- type parts of the junction, therefore there are several mechanisms that may limit the open-circuit voltage: the V_{OC} is most significantly affected by recombination of charge carriers, both surface and bulk [2]. A reduction in recombination increases V_{OC}. Recombination mechanisms are discussed in section 2.2.2.

An equation for V_{OC} in an ideal solar cell can be given as follows [3]:

$$V_{oc} = V_{bi} - \frac{A\mathrm{k}T}{\mathrm{q}} ln\left(\frac{\mathrm{q}pv_r}{J_L}\right) \tag{2.1}$$

where V_{bi} is the built-in voltage, A is an ideality factor, k is the Boltzmann constant, T is the temperature, q is the electron charge, p is the hole density, v_r is the recombination velocity and J_L is the photocurrent. The built-in voltage, a consequence of a $p-n$ junction, is related to the band gaps of the heterojunction materials and the band offsets, which are in turn determined by doping levels and carrier concentrations. The V_{bi} is the maximum value the V_{OC} can achieve. From equation 2.1 it can be seen that the V_{OC} is related to the built-in voltage, hole density, recombination velocity and photocurrent. Recombination within the space charge region causes a reduction in V_{OC} and FF [4]. Other factors that reduce the built-in voltage also reduce the V_{OC} such as reduced band gap or increased temperature.

The recombination of carriers in the depletion region has a negative impact on the V_{OC} as any minority carriers lost to recombination in this region must be resupplied by the external current. The current across the pn junction is the combination of carriers across the junction and this recombination current. It has been shown that reducing the recombination in the space charge region increases both V_{OC} and FF long before decreasing the reverse bias saturation current [5].

The photocurrent collection efficiency in CdTe cells has been linked to the field assisted transport of minority carriers in the depletion region in experimental studies by Hegedus *et al.* [6]. It was found that a uniform field $p-i-n$ model worked well for CdTe solar cells, and verified the assumptions of a nearly uniform field in the first micron of CdTe (where the bulk of the electron-hole generation occurs), and a linearly decreasing field beyond that. They speculated that voltage dependent collection reduces fill factor and V_{OC}, with depletion region recombination being the dominant loss mechanism.

b) J_{SC}

The short-circuit current occurs when the voltage across a cell is zero. It is the maximum current attainable from a solar cell. In an ideal cell the short-circuit current is identical to the light-generated current, J_L. Consequently the magni-

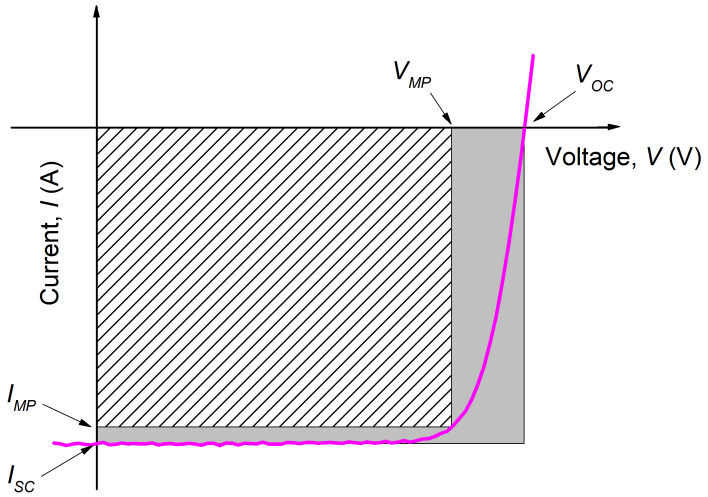

Figure 2.1: An example of an $I-V$ curve to demonstrate open-circuit voltage V_{OC}, and short-circuit current I_{SC}. The maximum power voltage V_{MP} and maximum power I_{MP} are used to calculate the fill factor FF, which is fraction of the shaded area to the grey area.

tude is dependent on the solar irradiance of the cell [7]. Any pathway that reduces the photon penetration into the semiconductor will reduce the J_{SC}. Hence losses occur secondary to reflection from and absorption in any glass layer, alongside absorption within the transparent conductive oxide (TCO) and cadmium sulphide (CdS) layers in a CdS/CdTe cell: carriers that are generated within the CdS layer are lost, whereas those generated within the CdTe layer are likely to be collected [8] - although the likelihood of carrier recombination before collection increases with distance from the junction [3].

The interaction of illumination with a cell can change the conductivity of the material resulting in an effect known as photoconductivity. This has been observed in CdS/CdTe cells [9] and attributed to the CdS layer. Blue light was found to significantly increase the depletion width and increase the quantum efficiency of red photons. The effect is thought to be secondary to the photoconductive CdS changing the electric field distribution which in turn effects the voltage dependent collection [6].

c) η

The efficiency of a solar cell is defined as the ratio of the electrical power output of a solar cell to the power of the incident light. It is calculated from parameters extracted from the $I-V$ curve (see figure 2.1). The parameter V_{MP} and I_{MP}

are the values of voltage and current at which the cell produced the maximum power, $P_{max} = V_{MP} \cdot I_{MP}$. The ratio of $V_{oc} \cdot I_{sc}$ to P_{max} is referred to as the fill factor, FF. Both the fill factor and efficiency η are defined below.

$$FF = \frac{P_{max}}{V_{oc} \cdot I_{sc}} \tag{2.2}$$

$$\eta = \frac{V_{oc} \cdot I_{sc} \cdot FF}{P_{in}} \tag{2.3}$$

where P_{in} is the input power from illumination. For standardisation purposes cells are tested under AM1.5 illumination providing $100\,\mathrm{mW/cm^2}$ at 25°C.

d) FF

The fill factor can be affected by recombination in the depletion region and hence an increase in the ideality factor A (see equation 2.1) and a decrease in V_{OC} [3]. The series resistance of the cell, R_S can also reduce FF, as can voltage-dependent current collection ($J_L(V)$) and shunt conductance G (the reciprocal of the shunt resistance, R_{SH}), as can be seen in equation 2.4 [3].

$$FF = FF_s\left[1 - \frac{(\zeta + 0.7)FF_s}{\zeta/(R_{ch}G)}\right] \tag{2.4}$$

where

$$FF_s = \frac{\zeta - ln(\zeta + 0.72)}{\zeta + 1}\left(1 - \frac{Rs}{R_{ch}}\right) \tag{2.5}$$

$$\zeta = \frac{qV_{oc}}{A\mathrm{k}T} \tag{2.6}$$

In these equations $R_{ch} = V_{oc}/J_{sc}$ is the characteristic resistance and R_s is the series resistance (discussed below). From equation 2.5 it can be seen that increasing the series resistance will have a detrimental effect on the fill factor as will a decreased shunt resistance [10].

Resistances

The efficiency of a solar cell is reduced by parasitic resistances. The most significant of these resistances are the series resistance R_S and the shunt resistance R_{SH}. The series resistance is in series with the main diode of the solar cell, and has several contributing factors. These can be divided into the contact resistances between metal contacts and the cell, and the bulk resistances of the semiconductor material and the contact/interconnect materials [11]. The shunt resistance is in parallel with the solar cell diode and is caused by leakage across the pn

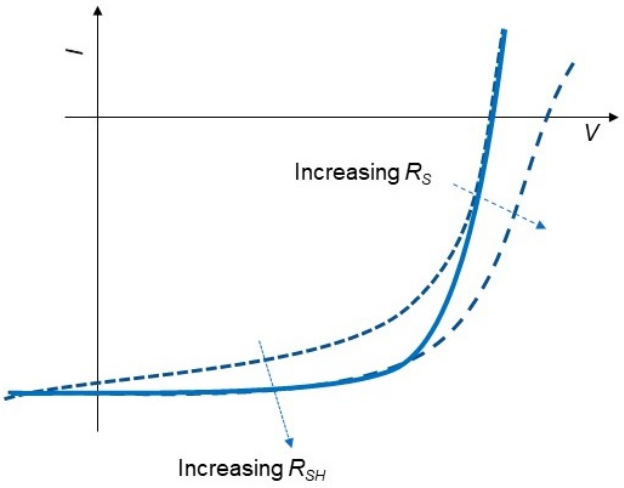

Figure 2.2: A diagram to demonstrate how changing R_S and R_{SH} affect the $I-V$ curve

junction or around the edge of the cell [2]. Both types of resistance can affect cell parameters, with the ideal solar cell having a low series resistance and an infinite shunt resistance.

2.2 Semiconductor defects, recombination and transport

2.2.1 Point and extended defects in semiconductors

Defects are always present in semiconductors. Any deviation in the crystal structure or local chemistry is regarded as a defect and has the potential to be damaging to the device, but may in the case of shallow dopant levels be critical for operation. Much of this thesis is concerned with 'trap' or 'recombination centres' which are deep levels in the band gap that arise from impurities, native defects (e.g. vacancies, interstitials or substitutionals) or some combination of the two, i.e. 'complex centres'. These may promote recombination by a number of mechanisms that are described in the next section.

In addition to point defects, extended defects may also promote recombination through capture of both holes and electrons, as occurs in Shockley-Read-Hall recombination (see below). Whereas traps delay the transport of charge carriers through semiconductors, recombination acts to remove the carrier altogether, and is therefore highly detrimental to solar cell operation. Deeper defects (closer to mid-gap) are more likely to act as recombination centres (see section 2.2.2.3), whereas shallower (closer to the band edge) defects are likely to act as dopants,

contributing holes or electrons to the lattice. (Some recombination centres can also act to generate charge carriers, and are termed generation-recombination centres [12].)

Examples of extended defects are stacking faults (a disorder in the crystallographic planes causing a planar defect), precipitates (areas of the crystal where, for example, there is an inclusion of a secondary state), and grain boundaries. Grain boundaries (GBs) may have wrong or disordered bonds, and may have a thin layer of foreign atoms 10 - 50 Å thick [13]. Twins are grain boundaries between grains having a special symmetric relationship.

For semiconductors with a low doping density, the presence of defects can increase the resistivity of the film, and thus influence the electrical behaviour of the material. The defects can also influence the local potential of the crystal and result in 'Fermi level pinning' at junctions.

2.2.2 Recombination mechanisms

To discuss the behaviour and characteristics of a photovoltaic device it is important to initially define some of the mechanisms occurring in a functioning device. Within a solar cell, incident radiation with an energy greater than the band gap E_g can be absorbed by excitation of an electron from the valence to the conduction band leaving a hole in the valence band. At the heart of a solar cell there is an electric field generated by a $p-n$ junction which serves to separate the electron and hole before recombination can occur. If the charges are generated in or near the space charge region[1] they are accelerated by the electric field which increases their thermal velocity by a drift velocity v_d (see equation 2.7). If a charge does not recombine before reaching the contacts it is able to leave the cell and contribute to the current [2].

$$v_d = \frac{1}{2}\frac{\mathrm{q}\tau_r}{m_e^*}\xi \tag{2.7}$$

The above equation gives the drift velocity of electrons where τ_r is the relaxation time (time between collisions - if this is averaged over all electron velocities the factor of 2 disappears from the above equation), m_e^* is the effective electron mass (incorporating the periodic force of the crystal lattice) and ξ is the electric field. The electron mobility is defined as $\mu_e = v_d/\xi = \mathrm{q}t_r/m_e^*$ and as such is related to the effective mass [2]. Similarly the hole mobility μ_p is defined as $\mu_p = \mathrm{q}\tau_p/m_h^*$ where τ_p is the relaxation time for holes and m_h^* is the effective

[1] The 'space charge region' is the region of the $p-n$ junction which is depleted of free carriers and in which the fixed dopant ion cores have an unbalanced charge, giving rise to the electric field of the junction.

mass of holes in the material [14]. The mobilities are related to temperature T and impurity concentration N through interactions between the charge carriers (electrons and holes) and phonons or impurities.

2.2.2.1 Radiative recombination

There are several main mechanisms by which electron and hole recombination can occur. The first is of these is radiative recombination. In this process an electron occupying an energy level higher than the thermal equilibrium level transitions to an empty lower-energy level. Most or all of the energy difference is emitted as light. This process is more rapid in direct band-gap semiconductors, as the transition there is a one-step process. In indirect semiconductors radiative recombination is a two-step process involving a phonon [2]. This leads to a lower radiative recombination lifetime in direct semiconductors compared to indirect semiconductors. Radiative recombination is present in high quality crystals and is, as such, unavoidable [15].

2.2.2.2 Auger recombination

In the Auger recombination process the energy difference between the energy states of the recombining electron is used to excite a second electron rather than being emitted as light. The second electron can be in the valence or conduction band, and returns to its original energy through phonon generation. This type of recombination is particularly important in low band gap semiconductors with high carrier densities, since the strength of carrier-carrier interactions is greater [15].

2.2.2.3 Shockley-Read-Hall recombination

Defect levels in the gap allow for a two-step recombination process as a (valence band) hole is captured by the defect, allowing an electron from the conduction band to recombine at the same defect. Thermal promotion of further holes to the defect allows the process to continue indefinitely. If the level is midway between the valence- and conduction-band edges this mechanism is particularly effective [2]. Recombinations of this type are known as SRH (Shockley-Read-Hall) events.

If a site mainly captures and releases one type of carrier only it is referred to as a trap, whereas it is called a recombination centre if it captures both carriers equally. As would be expected, recombination centres have energy levels deeper into the band gap where the density of electrons and holes is approximately

equivalent [15]. Where charges are trapped and later released the transport of carriers is slowed.

Am example of the complexity of these traps from impurities and defects in CdTe is shown in figure 2.8 later in this chapter on page 27. The recombination from these traps has a significant impact on the V_{oc} [16].

2.2.3 Transport in $p-n$ junctions

There are several mathematical descriptions of the flow of current through the $p-n$ junction (electrical transport) which correspond to different physical mechanisms. Experimental determination of the transport mechanism demonstrated by a device can be used to infer the nature of the electrical properties of the $p-n$ junction.

SRH recombination limited transport

A model was proposed in 1957 by Sah, Noyce and Shockley to describe $p-n$ junction $J-V$ behaviour of devices with single-energy, uniformly distributed SRH recombination-generation centres in the space charge layer [4]. The equation for this model is shown below (equation 2.8).

$$J = J_0\left(exp\left[\frac{\mathrm{q}V}{n\mathrm{k}T}\right] - 1\right) \tag{2.8}$$

where

$$J_0 = J_{00}\, exp\left(-\frac{\Delta E}{n\mathrm{k}T}\right) \tag{2.9}$$

It was later found that other models involving recombination in the depletion region could be described by the same equation [17]. An 'emission-recombination' model was proposed by Dolega, which described a highly distorted lattice at the $p-n$ junction with high recombination rates. The charge carriers would arrive at the interface through thermal emission. Unlike Sah, Noyce and Shockley's model, this model assumed a narrow region of defects at the interface and having a continuous distribution of energies. The key equation was later simplified to the equation below [18, 19]:

$$I = C\exp\left(-\frac{\mathrm{q}V_{bi}}{\beta\mathrm{k}T}\right)\left[\exp\left(\frac{\mathrm{q}V}{\beta\mathrm{k}T}\right) - 1\right] \tag{2.10}$$

where the constant C is weakly temperature-dependent, the value of β varies between 1 and 2, and V_{bi} is the built-in voltage. This is very similar to the

equation proposed in Sah, Noyce and Shockley's model above (equations 2.8 and 2.9).

When recombination dominates the transport at the junction, the value of ideality factor $n \approx 2$ such that the traps are localised near to the mid-gap and SRH recombination is most likely [1]. In Dolega's model, the reverse saturation current J_0 in equation 2.8 varies exponentially with voltage, whereas in Sah, Noyce and Shockley's model J_{00} is a constant, and

$$\Delta E = nV_{bi} \tag{2.11}$$

Multi-step tunnelling

The multi-step tunnelling model was proposed by Riben and Feucht [20]. Their assumptions included a large concentration of traps which are spatially distributed at the interface. Electrons tunnel stepwise from the conduction band through the band gap via these traps (which are assumed to be equally distributed in energy). The uniform distribution in space and energy allows calculation of the number of tunnelling steps, R, as is discussed below.

In a device which is dominated by multi-step tunnelling within the $p-n$ junction, it should be possible to express the forward current, J_f with the following equation [21];

$$J_f = J_0(T)\, exp(AV) \tag{2.12}$$

where

$$J_0 = J_{00}\, exp(BT) \tag{2.13}$$

In these equations J_0 is the saturation current, A is the gradient of lnJ vs V, J_{00} and B are constants, and V is the applied voltage. For multi step-tunnelling to be the dominant mechanism, the value of A should demonstrate a temperature dependence, although it is rarely found to be completely invariant in practice [22]. As J_0 is a function of temperature in this model, there should be a demonstrable exponential relationship between J_0 and T. Although there is no diode ideality factor n in this model, equation 2.12 can be used to estimate a value of n which towards room temperature is similar to that calculated with the 'single diode' equation (see Appendix B). As such, n can be a useful aid to diagnose this transport mechanism, as it should decrease with increasing temperature, although it does not have a physical meaning in multi-step tunnelling.

It is possible to use the dimensionless values of A to estimate how many tunnelling steps occur through the use of the following equations;

$$A = \alpha R^{-\frac{1}{2}} K \tag{2.14}$$

$$\alpha = \left(\frac{\pi^2}{2h}\right)\left(\frac{\varepsilon_p m_n}{N_A}\right)^{\frac{1}{2}} \tag{2.15}$$

$$K = 1 + \left(\frac{\varepsilon_p N_A}{\varepsilon_n N_D}\right) \tag{2.16}$$

For the last of these equations, for the cells studied in this work an approximation of $K \approx 1$ is used as the doping in CdS is several orders of magnitude greater than CdTe.

It is also possible to examine the reverse bias current, J_r for evidence of multi-step tunnelling using the equation below [23]:

$$ln\frac{J_r}{V} = ln\left(aq^2\frac{N_t}{h}\right) - \gamma\Big(V_{bi} - V\Big)^{-\frac{1}{2}} \tag{2.17}$$

If $ln\frac{J_r}{V}$ is plotted against $\left(V_{bi} - V\right)^{-\frac{1}{2}}$, a straight line should be evident, with the intercept related to the trap density required for tunnelling N_t.

Another feature of multi-step tunnelling can be determined from a log-log $J-V$ plot where

$$J_r \propto V^m \tag{2.18}$$

A negative slope of $\Delta m/\Delta T$ has been reported in CdTe devices and is thought to be further evidence of this transport mechanism [24].

2.3 CdTe and CdTe solar cells

2.3.1 CdTe solar cell design and performance

The semiconducting properties of CdTe were reported in the mid 1950s. The material quickly gained interest thanks to its band gap at the peak of the Shockley-Queisser graph for maximum efficiencies (see figure 2.3) [25]. Although Shockley and Queisser predicted a maximum possible efficiency of 33% for a device with the band gap of CdTe (1.45 eV) [26], that has been revised downwards to 29% in 1995 [27]. Further, more conservative estimates suggest 25% is the likely maximum *achievable* efficiency, when practical considerations are taken into account [28]. The current highest performing polycrystalline device has had a per-

formance of 22.1%, but was not able to match the high V_{OC} recently reported in monocrystalline devices ($>1\,\mathrm{V}$) [29, 30].

The simplest CdTe devices comprise four layers: a transparent conducting oxide (TCO) as the front contact (e.g. ITO or SnO_2:F, also known as FTO [flourine doped tin oxide]), a $\sim 100\,\mathrm{nm}$ layer of CdS, a 3 - 5 µm layer of CdTe and a (usually metal or graphite) back contact. Several other variations have been tested, with different materials or additional layers. The addition of a 'high resistivity transparent' (HRT) or 'buffer' layer between the TCO and CdS layers can improve performance [32] but also influences defect levels in the absorber [33]. The buffer layer's main function is to permit the use of thinner CdS layers, as it prevents shunting pathways through pinholes in the CdS (see next section). Common materials used for the buffer layer are metal oxides such as ZnO and SnO_2, which have band gaps $>3.2\,\mathrm{eV}$. The presence of a buffer layer can reduce the available light penetrating through to the CdTe through reflective losses, so the refractive index and thickness need to be optimised to maximise the optical response [34–36].

2.3.2 The CdTe solar cell: Materials, junctions and contacts

The components of the CdTe solar cell and the efficiency limiting factors are discussed in this section. An example of the calculated band structure for a typical unbiased device is shown in figure 2.4 with a $\sim 4\,\mu\mathrm{m}$ CdTe layer. (This differs from earlier band diagrams reported elsewhere which speculated the presence of a homojunction within the CdTe and a $p-i-n$ structure [37].)

The various interfaces are now discussed: firstly the heterojunction (CdS/CdTe

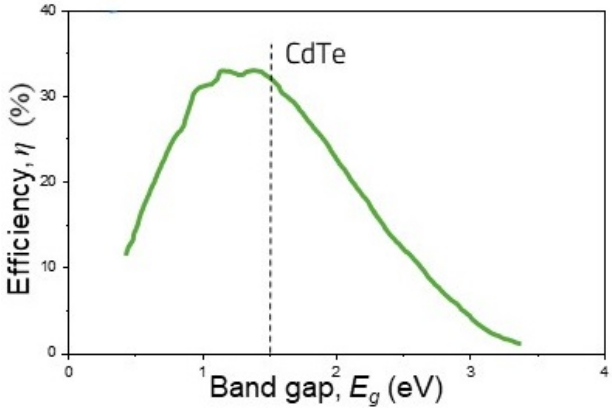

Figure 2.3: Shockley and Queisser's curve showing the variation of maximum possible efficient solar cell efficiency as a function of the band gap of the absorber [26, 31].

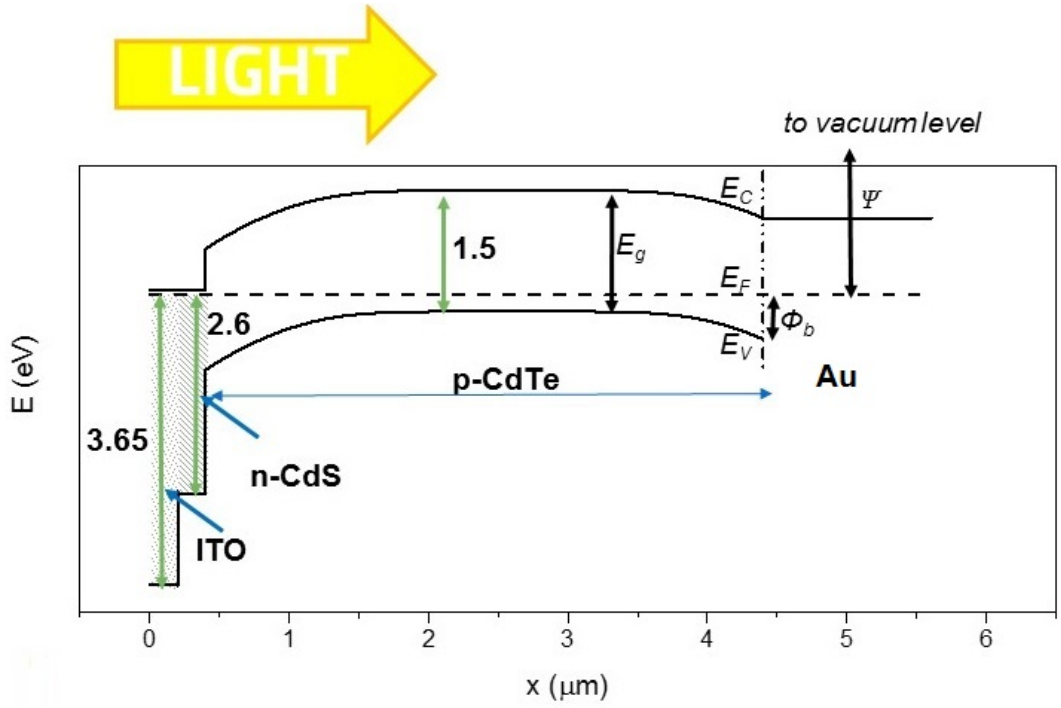

Figure 2.4: A simulation of the band bending in an ITO/CdS/CdTe device as calculated using the SCAPS software (a Solar Cell Capacitance Simulator) as developed by Burgelman *et al.* at ELIS, University of Gent [38].

junction) and 'window' layer (CdS in figure 2.4), then the front (ITO/CdS) and back (CdTe/Au) contacts.

2.3.2.1 Heterojunction and window

CdS layer

The precise nature of the function of this layer has been the subject of a great deal of study. Ostensibly as an n-type semiconductor it provides the 'n' part of the $p-n$ junction. However in practice that does not seem to be the case. Electron beam induced current (EBIC) studies have demonstrated that the depletion region is actually fully within the CdTe layer, albeit very close to the CdS [39].

Although CdS is a commonly used heteropartner to CdTe there is a 10% lattice mismatch between CdTe and CdS which results in a large number of defects at the interface. During post-growth processing intermixing can occur between the CdS and the CdTe, creating a $CdS_{1-y}Te_y$ alloy. This occurs both with high temperature annealing ($>500°$ C) and activation with $CdCl_2$, occurring to a lesser degree with thermal anneals prior to the activation process [40]. This is in part beneficial to the cell, as the lattice mismatch is reduced, although new defects are introduced in this process and the alloy has a lower band gap than either of the other materials. With over processing, the alloy can consume the

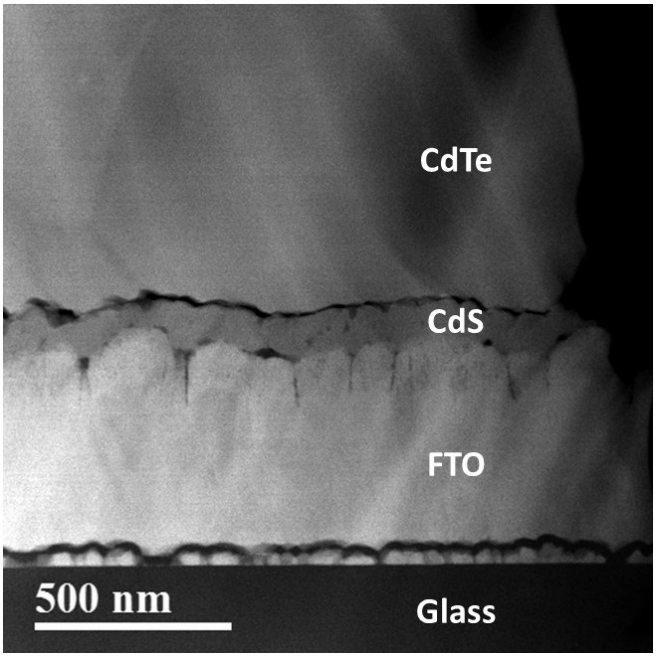

Figure 2.5: An scanning electron microscopy (SEM) image of a $MgCl_2$ processed CdTe device grown at Liverpool University by Dr. Jon Major. Image taken by Chen Li of Liverpool University, 2014. Flourine doped tin oxide (FTO) is used as the TCO in this device.

entire CdS layer, and contact directly to the TCO. This is detrimental to the cell, dropping both J_{SC} and V_{OC}.

The carriers excited in the CdS layer do not get collected by the external circuit, i.e. photons absorbed there are lost, and do not contribute to the generated current. This has been attributed to the low hole lifetime and high recombination in CdS [41]. This layer is also the first that significantly absorbs incident photons and it has a high absorption coefficient, so as its thickness increases, the higher the proportion of high energy photons are removed from the available spectrum. The band-gap of CdS is $\sim 2.4\,\text{eV}$, so photons $\lesssim 520\,\text{nm}$ can be absorbed. Consequently the CdS layer needs to be comparatively thin to prevent excessive J_{SC} lost to the cell. This can be difficult to optimize as during deposition it does not 'wet' the growth surface well, and thin layers can allow pinholes through to the HRT/TCO which permits a short-circuit if it connects with the CdTe layer after deposition. One mechanism to reduce the impact of this loss is to increase the band gap of the window layer, and therefore reduce the fraction of light withheld from the absorber layer. Interdiffusion between layers of Zn_2SnO_4 (ZTO, an alternative TCO) and CdS has been shown to have a beneficial effect on this parasitic absorption, thought to be secondary to Zn incorporation in the CdS layer [42].

There appears to be a minimum thickness of CdS required for good performance of the cell; approximately 60 nm for devices with a HRT layer, and 90 nm

for those without. Thinner layers start to reduce the V_{OC} [36].

CdS:O

Studies have demonstrated that the presence of O_2 during the sputtering of CdS allows the formation of CdS:O which can be beneficial for cell performance, in particular the J_{SC} [43–45]. The mechanisms of action are thought to be multi-factorial: the CdS:O films have higher optical band gaps (up to $\sim 3\,\text{eV}$ from $\sim 2.4\,\text{eV}$) possibly through the alloying of CdS with $CdSO_4$. The higher oxygen content of the films appears to suppress the Te diffusion from the CdTe into the CdS (which in turn produces a $CdS_{1\text{-}y}Te_y$ alloy which has a lower bandgap, and can be detrimental to the solar cell [46]). Additionally, the grain size of deposited CdS has also been shown to decrease with increasing oxygen during growth [47]. This is likely to improve coverage to the TCO layer, and reduce shunting losses though pinhole formation.

2.3.2.2 Contacts

The front contact is a transparent conducting oxide (TCO), such as FTO (SnO_2:F) or ITO (indium tin oxide, a solid solution of In_2O_3 and SnO_2) [48]. TCOs are highly doped conductive semiconductors with high band gaps ($\sim 4\,\text{eV}$). This property is thought to be related to a low conduction band minimum in these materials, such that the charge neutrality level lies within the conduction band [49]. They are largely n-doped, as p-doping has proven difficult to achieve with the same level of performance as n-type material [50]. TCO coated soda-lime glass of excellent quality is commercially available and commonly used for research lab solar cell manufacture. The band line-up as seen in figure 2.4 demonstrates the electrical compatability between ITO and n-CdS which allows for a low resistance front contact.

The back contact is however not so straight-forward. CdTe has a large electron affinity χ_s such that there are few materials with a large enough workfunction ϕ_m to make an Ohmic contact. Consequently, most metals, including the Au used in this work, form a Schottky contact with CdTe. A schematic of a Schottky contact is shown in figure 2.6.

The formation of a Schottky contact is as follows; when a metal and p-type semiconductor are contacted the charge carriers move to establish a flat Fermi level E_F across the junction. As the metal has significantly more charge carriers than the semiconductor, holes flow into the metal exposing negative cores, creating a strongly negative one-sided depletion region in the semiconductor. This creates a Coulombic repulsion to holes attempting to cross into the metal, im-

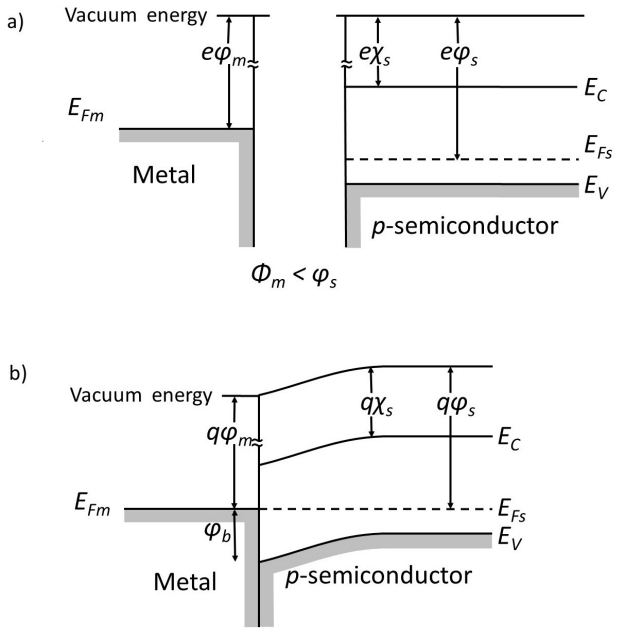

Figure 2.6: A schematic to show the band energies of a metal and a p-type semiconductor where $\phi_m < \phi_s$ a) before, and b) after being connected [51]: metal workfunction ϕ_m, semiconductor electron affinity χ_s, semiconductor ionisation potential ϕ_s, Fermi levels of metal E_{Fm} and semiconductor E_{Fs}, conduction band minimum E_C and valence band maximum E_V.

posing an energy barrier to be surmounted. This barrier, ϕ_b is shown in figure 2.6 b), and can be calculated in p-type materials using the equation below:

$$\phi_b = \frac{E_g}{\mathrm{q}} + \chi_s - \phi_m \tag{2.19}$$

where $E_g = E_C - E_V$ is the band gap of the semiconductor.

In the CdTe solar cell, the presence of this barrier at the back contact is detrimental to the performance, acting to drop the V_{OC} across the cell. The height of this barrier can be changed to some degree by processing of the device, as is described in the next section.

Back contact barrier height

The non-Ohmic behaviour at the back contact can be improved by creating a smaller Schottky barrier. Higher workfunction metals or other contact materials could reduce ϕ_b, but unfortunately few exist that are cheap enough to be practicable. Consequently Schottky contacts are frequently encountered in CdTe devices. It is possible to reduce the barrier by changing the stoichiometry of the CdTe at the back contact: increasing the p-doping would narrow the depletion width and the barrier height. One way this is achieved is through the use of acid etches on the back surface of the CdTe before deposition of the metal contact. These

acids preferentially dissolve the Cd atoms from the back surface, leaving behind cadmium vacancies which act as acceptors, creating an area of stronger doping. Ideally, sufficient doping would be possible to allow holes to tunnel through the barrier. Different etches have been studied and reported as having a greater impact on the barrier height than the metal used, with most values for ϕ_b in the range 0.55 - 0.6 eV [52–54].

The appearance of the $J-V$ characteristic curve under illumination is affected by the back contact Schottky diode, developing 'roll over' in high forward bias (see figure 2.7) [55]. This is a non-ideal situation, as under DC conditions the Schottky barrier acts as a diode reversed biased with respect to the CdS/CdTe junction, increasing the resistance and reducing solar cell performance [10, 56].

The presence of this second diode requires adaptation to the one-diode equation for solar cells (equation 2.20) by the addition of a second term (equation 2.21) [57]. In these equations I_{ph} is the light-generated current, I_0 is the reverse saturation current, with I_{01}, I_{02} as the terms for diodes 1 and 2 respectively, and n_1, n_2 are the ideality factors for each diode, both of which should take a value between 1 and 2. For CdTe devices the sign of one of the diodes in equation 2.21 is reversed with respect to the other, as they are acting in opposition [58]. However in situations where a high back-contact barrier is apparent and a pronounced roll over is evident in the I-V curve, advanced diode models may not be applicable, as solutions can give values for the ideality factors greater than 2 [59].

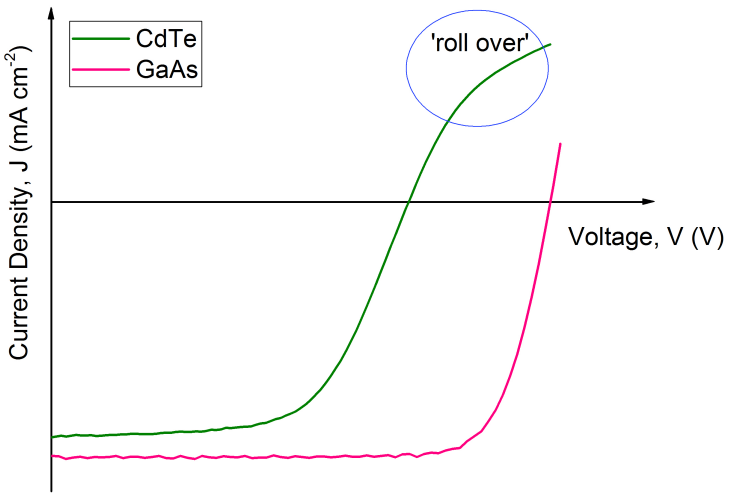

Figure 2.7: Comparison of the $J-V$ curves of a CdTe device with a GaAs cell to show the 'roll over' effect seen in forward bias in the CdTe cell.

$$I = I_{ph} - I_0\left[exp\left(\frac{\mathrm{q}(V + IR_s)}{n\mathrm{k}T}\right) - 1\right] - \frac{V + IR_s}{R_{sh}} \tag{2.20}$$

$$I = I_{ph} - I_{01}\left[exp\left(\frac{\mathrm{q}(V + IR_s)}{n_1\mathrm{k}T}\right) - 1\right] - I_{02}\left[exp\left(\frac{\mathrm{q}(V + IR_s)}{n_2\mathrm{k}T}\right) - 1\right] - \frac{V + IR_s}{R_{sh}} \tag{2.21}$$

Copper and doping

Copper is sometimes added to the back contact of CdTe devices to improve the Ohmic properties of the back contact, and increase the *p*-type doping by acting as an acceptor [60]. Even when it is not added intentionally, Cu often has a trace presence in other metals such as Au, and may be instrumental to the function of CdTe. However, CdTe is a difficult material to dope heavily as it demonstrates significant self-compensation, a feature that it has in common with other II-VI semiconductors [61]. Consequently an uncompensated acceptor density of $\sim 10^{16}\,\mathrm{cm}^{-3}$ is considered the upper limit of the normal range. This is demonstrated by considering how the intrinsic defects alter as the Fermi level changes. For cadmium rich material with *p*-type doping, the donor interstitial defect $\mathrm{Cd_i}^{2+}$ acts to compensate intentional acceptor dopants. In tellurim rich material a similar mechanism pins the Fermi level slightly closer to the valence band, producing *p*-type material. Usually as-grown CdTe is neutral or slightly *p*-type [62]. In the Te-rich regime there are no donor intrinsic defects which can form spontaneously when E_F approaches the VBM. However, there are numerous impurities in CdTe which can act in the self-compensation mechanism, such as Na or Cu for example.

Sodium donor and acceptor defects in CdTe limit its use as a dopant, as the defects have sufficiently low formation energies to form spontaneously irrespective of the local stoichiometry and act to self-compensate [63]. Copper is slightly different. It can act as a donor or an acceptor in CdTe depending upon its position in the lattice: a copper interstitial $\mathrm{Cd_i}$ acts as a donor, whereas a substitutional copper on a cadmium site $\mathrm{Cu_{Cd}}$ acts as a deep acceptor [64]. In Cd-rich conditions (*n*-type) copper acts to self compensate by forming $\mathrm{Cu_{Cd}}$, but in Te-rich conditions $\mathrm{Cu_{Cd}}$ has a lower energy of formation than the donor $\mathrm{Cd_i}$, so self-compensation should not happen. Although this makes Cu a likely acceptor dopant in CdTe it is not without problems: it is highly mobile and diffuses throughout the device, often collecting in the CdS to the detriment of the cell. Also it is a comparatively deep acceptor which would act to limit the hole density.

The stability of films with Cu added at the back contact has been studied,

with over-treated cells showing significant degradation with prolonged stress (60% reduction in FF after 1000 hours of stress) with Cu moving into the CdS [65]. PL measurements have suggested the presence of copper may create a comparatively shallow acceptor defect at 0.15 eV, but somewhat counter-intuitively act to limit hole lifetime [28]. A similar picture has been reported on simulated devices using SCAPS [66]. A positive effect has been reported however on the barrier height [67]. Suggested methods to improve the stability of the contacts include engineering polycrystalline CdTe in such a way that does not promote surface migration, for example with larger grain sizes [68].

2.3.3 Extended and point defects

Shallow doping in the CdTe is required for high performance. As has been mentioned above, copper is an acceptor dopant, but compensation is problematic. Some of the common extended and point defects seen are discussed here, with their potential impact on PV cell performance.

CdTe is prone to extended defects. It adopts the sphalerite crystal structure, but has a low stacking fault energy, such that stacking disorders and twins are common [69]. Polycrystalline CdTe films grown by closed space sublimation (CSS) have been found to contain a high number of stacking faults and lamellar twins [70], while dislocations and grain boundaries (GBs) have also been observed in chloride treated polycrystalline CdTe [71]. While these defects can cause deep states which promote recombination, grain boundaries can also be charged, and act to prevent current transport. It has been speculated that the extended defects are more damaging to CdTe device efficiency than point defects [72]. Theoretical calculations have been reported to show that stacking faults act as hole traps, reducing performance, while twin defects were reported to be electrically neutral and of little impact on performance parameters [73]. The numbers of stacking faults are however significantly reduced by annealing.

It has been reported that the resistivity of GBs limits the mobility of majority carriers across them [74]. Electrically active defects and wrong bonds at GBs create faults with deep level characters which therefore lead to recombination in as-grown material, and possibly electrical barriers [75]. However, numerous studies have demonstrated the GBs role as conduction pathways that are enhanced by the action of chloride processing (discussed in the next section). Following chloride treatment, Cl segregates to the GB and the local doping has been found to be n-type [76].

Point defects can also cause damaging recombination. In theory, shallow (< 0.05 eV above the valence band maximum, VBM) acceptors are needed to

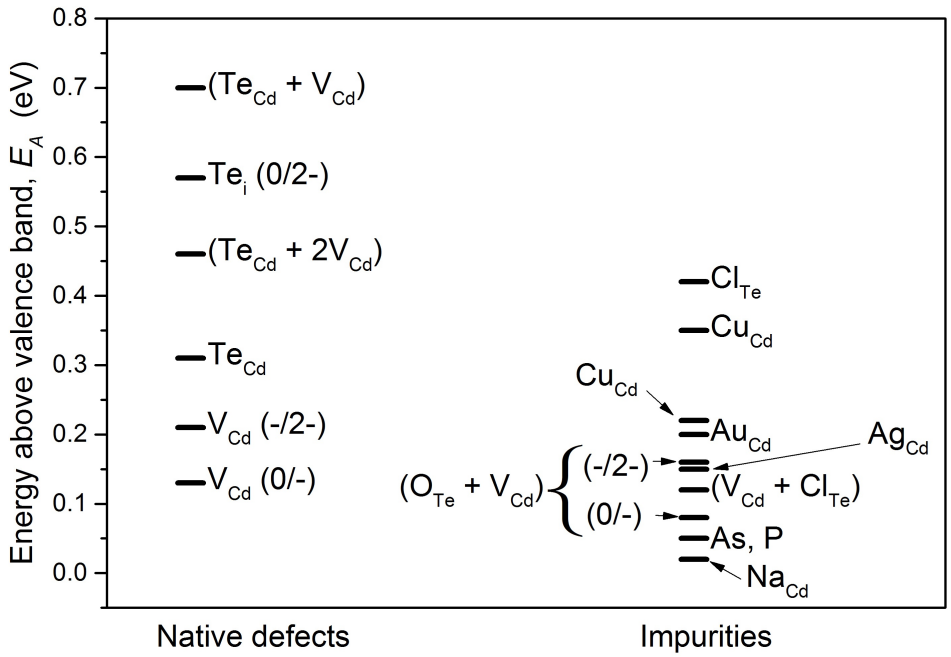

Figure 2.8: Energies of trap levels associated with native defects or impurities in CdTe devices [62, 78–83]. Energies are above the valence band, and only hole traps are included.

become ionised at the operating temperature of the device, but many potential dopants produce deep acceptor levels. There are several reported point defect levels in the CdTe band gap, with some in the mid-gap region. These are very likely to act as recombination centres through SRH processes. Shallower defects (0.05 - 0.5 eV above VBM) also cause recombination, and act to reduce V_{OC}. A number of point defects have been associated with specific chemical complexes, and are shown in figure 2.8. They include the so-called 'A centre', the cadmium vacancy substitutional chlorine (V_{Cd} + Cl_{Te}) acceptor complex, which is speculated to improve shallow doping, as it is slightly shallower than the V_{Cd} defect [62, 77, 78]. The substitutional Cu defects are also of interest later in this work and are seen at activation energies of 0.22 eV for the first ionisation (0/-) and ~0.35 eV for the second (-/2-)[2]. Despite their deep nature, they are thought to act as acceptors, but are not fully ionised at room temperature.

.

[2]The notations of (0/-) and (-/2-) indicate the charge states of the trap associated with an activation energy - for the first ionisation the charge state changes from neutral (0) to singly negative (-).

2.3.4 Chloride processing and activation

Post-growth processing became commonplace following its introduction in the 1980's by Basol [84, 85]. Prior to this, spray pyrolysis was used to produce CdS layers using a $CdCl_2$ and thiourea solution [86]. As-grown CdTe devices produced without the use of a $CdCl_2$ flux had low efficiencies, but upon annealing these improved to $< 10\%$. When treated with $CdCl_2$ after growth, by annealing a sample in the presence of $CdCl_2$, improved efficiencies were possible, and alternative growth mechanisms of p-type layers became more practicable. In 2000 Barth *et al.* patented an apparatus to allow for mass production of CdTe modules which combined CdS depoition, CdTe deposition and $CdCl_2$ treatment [87]. This process, with modifications, is still in use today. The current effects of chloride treatment are discussed below, through the effects it has on performance, the physical effects on the cells, and the current understanding of why it works.

Effect on performance

- The effect of $CdCl_2$ can be profound, and exceed the reported benefits from annealing alone. As-grown CdTe devices are commonly found to have efficiencies of $< 1\%$. Annealing typically produces devices $\ll 10\%$, whereas annealing in the presence of $CdCl_2$ transforms an as-grown cell to a device with $> 10\%$ efficiency [23, 88].
- The performance improvement is evident across all parameters measured by the $J-V$ curve, i.e. V_{OC}, J_{SC} and FF. All these parameters are improved by annealing alone, but not to the same degree.
- Quantum efficiency is also increased, particularly for longer wavelength photons [89].
- A comparison of different chloride salts demonstrated that best efficiencies were possible with chlorides possessing lower bond dissociation energies, suggesting the Cl^- ion is the critical aspect. $CdCl_2$ and $MgCl_2$ produced the highest values of η and V_{OC}, and demonstrated increased Te-rich stochiometry at the back contact, potentially reducing the Schottky barrier. [90]

Effects of over-treatment

- Physical changes occur in devices with over-treatment of $CdCl_2$ which have been thought to relate to the build-up of Cl at the CdS/CdTe interface [91]. These correspond to deterioration in performance. Prolonged annealing time has similar effects, where increasing improve-

ments to the crystal microstructure are outweighed by the chlorine build-up.

Effects of oxygen

- Although annealing in air is beneficial for CdTe devices, a build up of Te oxides on the exposed back surface is deleterious to device performance, which can return to the as-manufactured efficiency levels after chemical etching of the oxide layer [92]. However, the presence of oxygen during close space sublimation (CSS) CdTe deposition appears to have mixed effects - through decreasing grain size it has the action of increasing grain boundary density, negatively affecting hole mobility, but also improving shallow doping, possibly though the formation of (O_{Te}+V_{Cd}) shallow acceptors.

Underlying physical effects

- **Recrystallisation** - there are a number of reports about the degree of recrystallisation in CdTe. The reported observations have been shown to depend on the deposition method of the CdTe layer. In layers where there is considerable stress, (e.g. physical vapour deposition [PVD] films, or sputtered films) there is strong evidence of recrystallisation and grain growth, whereas in less stressed layers (produced through close space sublimation [CSS] for example) this does not occur [93,94]. X-ray diffraction (XRD) of (PVD deposited) as-grown CdS/CdTe devices has demonstrated polycrystalline material with a mix of cubic and hexagonal structures. Following treatment with $CdCl_2$ this was found to change to exclusively cubic structures, with a preferred (1 1 1) orientation and larger grain sizes [95]. Other PVD grown films have however found slightly different results. As-grown films were highly-strained, with mixed hexagonal and cubic CdS, and single-phase columnar CdTe pseudo-epitaxially grown on top. On annealing without $CdCl_2$ the interface strain was somewhat relaxed, thought to be through a small degree of interdiffusion at the heterojunction, and an increased randomness was observed in the preferred orientation of crystal structure. Brief annealing (2 minutes at 550 °C) did not affect the columnar grains or micro-twins [96]. Annealing in the presence of $CdCl_2$ induced grain growth and recrystallisation within 10 minutes of processing (at 415 °C) [97]. Later work by the same team found similar results, with the most random orientation but least progressive recrystallisation and grain growth in samples subject to a high temperature

anneal (30 minutes at 550 °C) prior to chloride treatment [40].

Other findings have been reported, with conductive tomographic atomic force microscopy not demonstrating recrystallisation in $CdCl_2$ treated devices, but with changes to the electrical behaviour of the grains and grain boundaries. This will be discussed further shortly.

- **Minority carrier lifetime** - This is important for solar cell devices, the operation of which depends on injection of minority carriers [14]. $CdCl_2$ treatment has been reported to increase the lifetime in CdTe devices *whether or not* the crystalline quality improved [93]. This implies that the minority carrier lifetime has dependencies on factors unrelated to crystal quality.
- **Intermixing at heterojunction** - When annealing is undertaken without $CdCl_2$, there is some interdiffusion of S into CdTe and Te into CdS. In the presence of $CdCl_2$ the progression of S diffusion into CdTe is increased [40, 97]. However, the diffusion of Te into CdS is reduced in $CdCl_2$ treated devices [98]. Cl has been found to accumulate at the CdS/CdTe boundary, with S diffusing along grain boundaries. Optimal $CdCl_2$ treatment has been reported to promote the formation of a thin layer of CdS_xTe_{1-x} alloy at the interface, which is absent in over-treated devices [89].
- ***p*-type doping** - Treatment with $CdCl_2$ has been reported to coincide with an increase in *p*-doping, particularly towards the junction [99–101]. This may be through the introduction of deep acceptors, rather than the interdiffusion of species [102].
- **Charge carrier transport** - Multi-step tunnelling has been found to be the dominant transport mechanism in as-grown and annealed cells, changing predominantly to a thermally activated mechanism in chloride treated devices [23, 103]. The presence of interface states has been reported with both $CdCl_2$ and $MgCl_2$ treatment, with a lower density in the latter. The series resistance R_S has also been found to decrease as a result of treatment, which is speculated to indicate the passivation of interface states.
- **Effect on grain boundaries** - Although theoretical work suggests the majority of Cl is to be found within crystal grains after $CdCl_2$ treatment, there is strong evidence of Cl accumulation in GBs [71,104]. There have been observations of continually changing deep levels as a function of degree of $CdCl_2$ processing which has been theorized to be related to grain boundary passivation [105]. Investigations using (CT-

AFM) have also found that Cl treatment allows intra-crystal planar defects to act as conductive pathways for holes, which are described as being spatially and energetically orthogonal to the grain boundaries. The GBs themselves were noted to act as n-type corridors. These findings were absent in non-chloride treated samples [106]. This is similar to other work by Tuteja *et al.* [107] which demonstrated that the GBs dominate current flow in forward bias, with reduced p-type doping along GBs and increased current across grains compared to as-grown cells. The action of $CdCl_2$ to passivate grain boundaries was also discussed by Edwards *et al.* [108] who also found evidence of a current in the GBs after treatment. Other groups have measured the grain boundary barrier height through $J-V$ measurements in low injection conditions, and concluded that this barrier height increased with $CdCl_2$ activation.

- **Effect on deep levels** - Lourenço *et al.* reported a continuously varying trap level with increasing $CdCl_2$ treatment. The decreasing trap level correlated with an improvement in efficiency. The measured trap was speculated to be trap related to, or situated in the grain boundaries [105].

- **Effect on CdTe grain size**

  There are a number of literature reports of the effects of annealing CdTe thin films in the presence of $CdCl_2$, some of which report grain growth and others not [93]. Moutinho [109] and later Cousins ([110] provide a systematic framework for understanding the various experimental observations in terms of the classical metallurgical processes of recovery, recrystallisation and grain growth. Originally developed to explain phenomena in cold-worked metals, the same energetic drivers for structural change have been invoked to give satisfactory explanations of the behaviour of faulted and polycrystalline semiconductors, as discussed below.

  For heavily faulted materials, the volume strain of the material drives the first two processes i.e. i) recovery, during which dislocations and planar faults reorganise and decrease in density to generate identifiable grain boundaries, ii) recrystallisation during which the overall volume strain is reduced by the formation of new grains which originate from the interstices of the old ones, and which eventually take over the whole volume of the film. When the grain structure is fully established a slower process of grain growth (iii) takes place in which

the total energy per unit area of the grain boundaries is minimised by the expansion of grains. For the case of small grained CdTe thin films, Moutinho *et al.* [109] used Nelson-Riley precision lattice parameter measurement and Harris crystal texture analysis to demonstrate that process (ii) was operating so as to generate a second population of low-strain grains which had random orientation in contrast to the oriented texture of the as-grown film. Moreover, Moutinho went on to demonstrate that the extent to which the processes of recrystallisation and grain growth took place depended solely on the state of the material before annealing, rather than the growth method: small grained material (e.g. 100 nm) with strain underwent recrystallisation and grain growth while for material for which the grains were already large (e.g. $> 0.5\,\mu m$) and had low strain, there was neither recrystallisation nor grain growth.

Cousins *et al.* [110] demonstrated that for close space sublimation-grown CdTe, the grain size distribution in the film was unchanged by chloride annealing, even for extended periods of time up to 60 mins, this representing extreme 'overtreatment'. This is consistent with the material having been grown at a comparatively high temperature (550Â°C) and its already large grains. For the studies conducted in this work the CdTe layer are grown by close-space sublimation (CSS). Figures 2.9 a) and b) show that the grains in this CSS-grown material are similarly large to those studied by Cousins (typically $> 0.5\,\mu m$). Therefore absence of grain growth in these samples is fully expected in accordance with Mouthino's framework.

The use of $MgCl_2$ as an alternative to $CdCl_2$ has begun to attract research effort, but as yet has not produced record efficiencies. It remains to be seen whether this is simply secondary to the relative lack of time spent on studying this processing method, or if there is an intrinsic limit to the benefits achievable with $MgCl_2$.

2.3.4.1 Effects of $CdCl_2$ processing on the equivalent circuit model

The extent of chloride treatment has a profound effect not only on the performance of CdTe PV devices, but also the AC equivalent circuit that describes them. A good example is provided by Major *et al.* [111], who investigated the effects of chloride treatment,compared to devices having insufficient chloride. The two groups of devices were each represented by radically different equivalent circuits as follows;

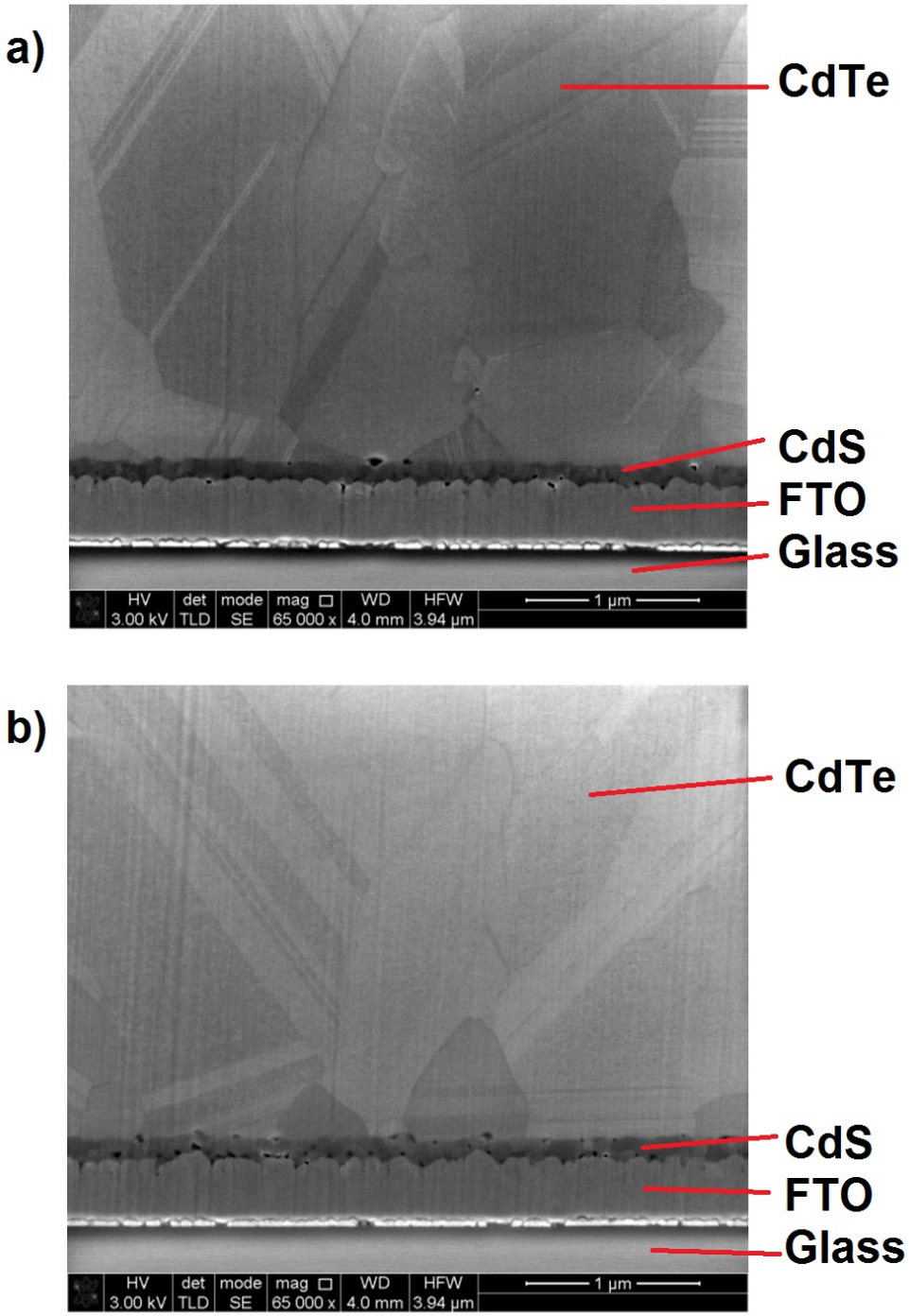

Figure 2.9: Scanning electron microscopy (SEM) images of CdTe devices grown by close-space sublimation (CSS) by Dr. Jon Major. Fig a) and b) show SEM cross-sections of the microstructure of CdTe films grown and chloride treated under similar conditions to the ones explored in this work, both in the as-grown state (fig a) and after chloride treatment with $MgCl_2$ (fig b). Overall the grain size distribution (0.5 - 1 µm) is largely unchanged by the chloride anneal for these samples. Images taken by Chen Li.

a) For the cells prepared without sufficient $CdCl_2$, equivalent circuit analysis required three RC components as shown in figure 2.10. The first (R_0C_0) segment represented the back contact Schottky barrier and the $R_1 - CPE_1 - CPE_2$ component to account for the contribution from the main $p-n$ junction. The third RC section was connected to the presence of grain boundaries, as the values varied in a series where the CdTe grain size was the only variable, with lower values of R_2 and C_2 in the devices with largest grains.

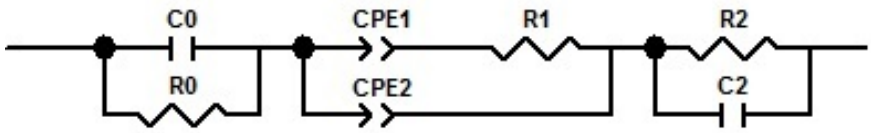

Figure 2.10: Equivalent circuit model of an unetched device [111].

b) In contrast, similar samples which had sufficient $CdCl_2$ treatment could be described by a much simpler circuit at different DC biases and varied levels of illumination (see figure 2.11). The RC section accounting for the grain boundary contribution was no longer needed, with the back contact resistor R_S becoming much smaller ($\sim 20\,\Omega$) with no associated capacitance.

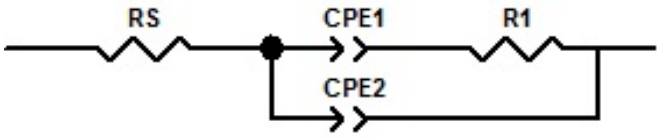

Figure 2.11: Equivalent circuit model of an etched device [111].

Other studies conducted by Proskuryakov *et al.* explored equivalent circuit models for CdTe cells in various states of processing [100, 112]. These models and their interpretation are discussed in section 4.3.4.3.

2.4 Opportunities and unknowns for CdTe solar cells / Scope of this thesis

There are three main areas of focus of this thesis. Firstly, and most importantly, is the observation of electrical parameter variation with $MgCl_2$ processing, and comparison with $CdCl_2$ treated devices. Secondly, the separate effects of simple thermal annealing and chloride processing are explored, to identify how they individually affect performance. Finally the focus is shifted towards shallow doping,

with an alternative material for copper introduction, i.e. a copper thiocyanate back contact. Across these studies there are opportunities to examine factors which act to improve the V_{OC} of studied devices, with a particular focus on deep and shallow trap behaviour.

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3. Experimental methods used in this work

3.1 Scope of this chapter

In this chapter the fundamental theory behind the experimental techniques is described with reference to CdTe as appropriate. The experimental details themselves are presented in chapter 4.

3.2 Current-voltage based methods

One of the simplest and most common experiments is to supply a voltage across a solar cell, and measure the resulting current. Dark readings in CdTe can vary from light readings, as the CdS is photo-conductive. This changes the DC series resistance, and is postulated to be the cause of 'crossover', a phenomenon where the light and dark curves cross each other in forward bias (in the voltage range dominated by R_S) [1, 2].

3.2.1 Current-voltage performance under illumination

This is used to obtain the $J-V$ curve as discussed in section 2.1, and determine the parameters V_{OC}, J_{SC}, FF and η. To provide a standardised test, a light source supplying an AM1.5 solar spectrum at $1000\,\mathrm{W\,m^{-2}}$ is used. This is usually provided by a halide light source with a spectral filter designed to mimic the insolation at sea level (through an air mass equivalent to 150% times the equatorial value).

Useful information can be gleaned from illuminated $J-V-T$ studies including values for the built-in voltage, V_{bi}, and evidence for transport mechanisms. Plotting the V_{OC} as a function of T can provide an estimate of V_{bi} through the

following equation:

$$V_{OC} = \frac{n\mathrm{k}T}{\mathrm{q}} ln\left(\frac{J_{SC}}{J_0}\right) + V_{bi} \tag{3.1}$$

A straight line plot should be produced with the intercept at $T = 0$ at the value of V_{bi} [3].

Illuminated current-voltage studies as a function of temperature ($J-V-T$ studies) at different light intensities can also provide an improved estimate for the diode factor n [4]. This value can aid the interpretation of dominant transport mechanisms (as discussed in chapter 2.2.3). Taking $J-V$ measurements at two different light intensities, 'a' and 'b' can allow plotting of the following equation, from the gradient of which n can be calculated:

$$V_{OC}(a) - V_{OC}(b) = \frac{n\mathrm{k}}{\mathrm{q}} T ln\left(\frac{b}{a}\right) \tag{3.2}$$

3.2.2 External quantum efficiency

The external quantum efficiency (EQE) of a solar device is a ratio of the number of carriers collected by the external circuit to the number of photons incident on it. There are a number of loss mechanisms that are not related to the quality of the $p-n$ junctions, such as reflections from the glass, transmission across boundaries with a change of refractive index, and absorption in layers outside the depletion region. Other quantum efficiency losses can occur through the loss of generated charge carriers through recombination. When the external quantum efficiency is measured as a function of wavelength, the spectrum shape may be used to diagnose performance features such as window absorption. The area under the EQE can be used to determine the J_{SC} of the device independently of $J-V$ measurement.

3.2.3 Temperature dependent current-voltage measurements

The variation of current density of a device with applied voltage can be studied as a function of temperature in ($J-V-T$) experiments. Analysis of the changing shape of the curve can elicit information about the transport properties of charge carriers through the cell, including conductivity types and back contact barrier height as described in the following sections.

Back contact barrier height

The height of the Schottky barrier at the back contact of the device can be measured through $J-V-T$ data. Bätzner *et al* demonstrated that for CdS/CdTe devices, the series resistance R_S changed as a function of temperature in a manner which could be described by equation 3.3 [5]. This equation consists of three parts, the first two of which describe an Ohmic response, and the third an exponential relationship. The exponential section describes thermionic emission over the back contact Schottky barrier.

$$R_s = R_{\Omega 0} + \frac{\partial R_{\Omega 0}}{\partial T}T + \frac{C}{T^2}exp\left(\frac{\phi_b}{\mathrm{k}T}\right) \tag{3.3}$$

In the above equation $R_{\Omega 0}$ is the resistance at 0 °C, $\partial R_{\Omega 0}/\partial T$ is the Ohmic temperature coefficient, C is a fitting parameter and ϕ_b is the height of the Schottky barrier. The exponential section of this equation is dominant in controlling the shape of the curve, and fitting the third part of the equation only has been reported to provide reliable estimates for ϕ_b [4].

Current transport

Dark $J-V-T$ data can provide evidence for current transport mechanisms as described in section 2.2.3. The methodology used in this work was to examine the data for evidence of multi-step tunnelling first, using equation 2.12. Demonstration of independence of A with T, decreasing J_0 with T, and increasing n with T (calculated using equation B.1 in Appendix B) was considered preliminary evidence of multi-step tunnelling. (Although A should be invariant with T [6], it is often found to have a slight temperature dependence [7, 8].) The data was then examined in reverse bias using equations 2.17 and 2.18. Only if features of multi-step tunnelling were found in all cases was this considered to be the dominant transport mechanism.

For data sets which did not provide good fits with 2.12 or the tunnelling model, attempts to fit the data to the single diode equation (equation 3.4 below) were made to improve the estimate of n. This is discussed further with reference to Series 521 in section 5.3.1.2.

$$J = J_0\left(exp\left[\frac{V-(JR_s)}{n\mathrm{k}T}\right]-1\right)+\frac{V-(JR_s)}{R_{sh}} \tag{3.4}$$

3.3 Capacitance methods and AC methods

3.3.1 Overview

For the interpretation of capacitance-voltage ($C-V$) analysis, or capacitive frequency response analysis (FRA) it is critical to have some understanding of the junction under study. There are a number of assumptions and approximations that can be made to simplify the calculations, and their validity is critical to the meaningfulness of the results and interpretations. $C-V$ analysis in all its forms allows analysis of doping density, defect centres and deep electrical states [9], and is also widely used to study thin film solar cells including CdTe [10–14]. However, the assumptions and approximations must be examined for validity prior to interpretation of the results. This section examines these and their applicability to CdS/CdTe devices.

3.3.2 Capacitance-voltage methods

Capacitance-voltage ($C-V$) analysis can be used to determine the uncompensated carrier density of $p-n$ junctions and Schottky barriers. At its core is the assumption that the junction behaves in a similar manner to a parallel plate capacitor. This involves several assumptions and approximations which make up the 'depletion approximation' as follows;

(a) The semiconductor can be split into two distinct regions, where one is the (completely) carrier-depleted space charge region.

(b) The second region is the bulk, which is electrically neutral.

(c) There is an abrupt boundary at each edge of the space charge region, and this defines the depletion width W_D

Further assumptions used in the derivation of the $C-V$ relation in equation 3.5 are:

- The depletion width is entirely contained in the weakly doped material (a 'one sided' junction)
- The doping is uniform
- There is no charge at the interface itself e.g. from dangling bonds

- The free carrier density is given by Boltzmann statistics (when $E_F - E_V > 3\mathrm{k}T$);

$$p = Nv\, exp\left(- \frac{E_C - E_F}{\mathrm{k}T} \right)$$

- Under reverse bias, the local carrier density in the space charge region is determined by the 'quasi-Fermi level' using the equation above.

- Dopants are fully ionized in neutral material

When these assumptions are true, Poisson's equation has been used to demonstrate the following relationship [9];

$$C^2 = \frac{\mathrm{q}\varepsilon\varepsilon_0 N(W)}{2(V - V_D)} \tag{3.5}$$

where C is capacitance per area, V_D is the diffusion voltage and $N(W)$ the net space charge density at the edge of the depletion region.

For such an ideal junction, a plot of C^{-2} as a function of V should be a straight line in reverse bias, with a gradient proportional to $N(W)$ and an intercept on the x-axis of $(V_{bi} - V_D)$, where V_D is related to the band bending of the Fermi level E_F [9, 15]. The frequency at which the analysis is performed has an important effect on the results: at low frequencies, the traps in the depletion region are able to contribute to the capacitance, whereas at high frequency inductive resonances can create anomalies [16], alongside interference from the back contact of the device. A high enough frequency should be chosen such that the deep levels are no longer able to respond, and therefore do not contribute to the device capacitance, yet a frequency which is not so high as to develop resonant artefacts. In practice this can be determined by finding the frequency at which the curve shape begins to rapidly change in characteristic from the low frequency to high frequency regime. For the majority of devices studied here this change occurred between 0.1 - 0.5 MHz.

CdS/CdTe devices are not ideal solar cells, and do not obey all the assumptions stated above. They are often treated as single-sided junctions, as the doping level in the CdS is many orders of magnitude greater than in the CdTe [17]. The junctions are not abrupt, nor the doping homogeneous, so it is common for $C-V$ analysis to demonstrate non-ideal behaviours. However equation 3.5 is still used for CdTe cells, which can create difficulties in interpretation. This is discussed further in Appendix C.

3.3.3 Thermal admittance spectroscopy

Thermal admittance spectroscopy (TAS) is a materials characterisation technique that is a subset of the impedance spectroscopy (IS) methods. In is broadest forms IS can probe the behaviour of mobile or fixed charges, and can be applied to solids and liquids, from dielectrics to metals [18]. In semiconductors, TAS has been used to determine defect energy distributions through the measurement of junction capacitance [19]. The equations used in this work, with some description of their origin, are detailed here, and demonstrated with a worked example shown in Appendix A.

Experimentally, TAS uses a frequency dependent change in AC conductance to measure the energy of the defect responsible for the change. A low amplitude AC voltage is applied across a sample (the 'test signal') and the admittance of the sample is determined through separate measurements of conductance G and capacitance C (see table 3.1). The admittance changes as the frequency of the test signal is varied. The 'peak frequency', f_p ($\omega_0 = 2\pi f_p$) at which admittance change occurs reduces with reducing temperature (T). Through population of an Arrhenius plot with ω_0 and T data, an energy can be calculated. This experimental technique studies thermal emission from defects. As defects capture charge carriers, at low frequency ($\omega < \omega_0$) the defect can follow the test signal, and is able to charge and discharge and therefore contribute to the capacitance of the junction. As ω is increased above the defect's thermal emission rate, at which point it can no longer match the signal, it no longer contributes to C which therefore decreases. This is the reason for using high frequency data for $C-V$ analysis as discussed previously. It is important to note that no illumination is required, as the AC signal will discharge the traps during one half of the AC signal cycle and charge during the other.

Series circuit		**Parallel circuit**		**Relationship**
Impedance	$Z = R + iX$ [Ω]	Admittance	$Y = G + iB$ [S]	$Z = \frac{1}{Y}$
Resistance	R [Ω]	Conductance	G [S]	$R = \frac{1}{G}$
Reactance (capacitive)	$X_C = \frac{1}{\omega C}$ [Ω]	Susceptance (capacitive)	$B_C = \omega C$ [S]	$X_C = \frac{1}{B_C}$

Table 3.1: The reciprocal relationships between impedance and admittance terms (inductive reactance and susceptance have a similarly reciprocal relationship to each other, but are not considered here). In electronics the left hand or right hand terms are used to simplify the combination of circuit elements for series or parallel circuits respectively.

In frequency response analysis (FRA) data for conductance and capacitance is usually collected simultaneously. As demonstrated in table 3.1 these two are connected through Kronig-Kramers relations, meaning that they are the real and imaginary part of a complex function. They both contain the same trap information. However, they can be measured in different ways. The conductance is related to the energy loss from the test signal, caused by the phase shift that occurs though the capture and emission of charge carriers by traps. The capacitance is measured from a change in capacitance, as it is a parallel measurement. Their accuracy and sensitivities may therefore be different [20]. Using both to calculate trap energies independently of each other increases confidence in the results.

Not all traps in the band gap contribute to the junction capacitance equally. As a small AC signal is used in TAS, there is only a small fluctuation in the quasi-Fermi level which allows the filling and emptying of traps. Consequently, it is only traps with activation energies close to the Fermi level that will contribute to the capacitance (under the assumption that the density of trap states N_t is approximately constant around $E_F \pm 2\mathrm{k}T$). This leads to a relationship between C (the imaginary part of the admittance) and $N_t(E_F)$, where:

$$C = q^2 \frac{\widetilde{u}_p}{\widetilde{u}_{ext}} N_t(E_F) \tag{3.6}$$

In equation 3.6 $\widetilde{u}_p$ is the local band-bending of the quasi-Fermi level due to the applied AC signal, and $\widetilde{u}_{ext}$ is the applied external signal. For a continuous energy distribution of traps within the band gap, this equation would be dominated by traps close in energy to E_F, if the angular frequency was low enough for the traps to respond.

In the $p-n$ junction, the energy position of the Fermi level with respect to the valence band maximum is related to the physical position x within the depletion region W. Using the Fermi level in the n-type bulk, E_{Fn}, as a reference point, this position can be represented as follows;

$$E = E_F = E_{Fn} - \frac{x}{W}\mathrm{q}V_{bi} \tag{3.7}$$

As there is an assumed distribution of energy states, equation 3.6 needs to be integrated across the energy range. This is undertaken by integration with respect to space (which is equivalent to integration with respect to energy in this case, as the distance between the defect [at the Fermi level] and the band edge depends on the position within the junction as seen in equation 3.7):

$$C = \frac{q^2}{\widetilde{u}_{ext}} \int_{x_1}^{W} \widetilde{u}_p(x) N_t(E_F(x)) dx \tag{3.8}$$

$$= -\frac{q^2}{\widetilde{u}_{ext}} \int_{E_0}^{E_{Fp}} \widetilde{u}_p(x(E)) N_t(E) \frac{W}{qU_d} dE \tag{3.9}$$

In the above equations, x_1 is the point in the depletion region where the trap energy, E_0, and the Fermi level crosses, and E_{Fp} is the Fermi level in the p-type bulk. When the external signal oscillates at $\omega = \omega_0$, the maximum frequency signal at which a defect with energy E_0 is able to be charged and discharged (and therefore contribute to the junction capacitance):

$$\omega_0 = 2\beta_p N_V \, exp\left(-\frac{E_0}{\mathrm{k}T} \right) \tag{3.10}$$

and therefore

$$E_0 = \mathrm{k}T ln \frac{2\beta_p N_V}{\omega} \tag{3.11}$$

where β_p is the hole capture coefficient and N_V is the density of states in the valence band. With the assumption that $\widetilde{u}_p = \widetilde{u}_{ext}$, and the use of the chain rule:

$$\frac{dC}{d\omega} = \frac{dC}{dE_0} \frac{dE_0}{d\omega} \tag{3.12}$$

and

$$\frac{dE_0}{d\omega} = -\frac{\mathrm{k}T}{\omega} \tag{3.13}$$

Walter *et al* [19] demonstrated that

$$N_t(E_\omega) = -\frac{V_{bi}}{\mathrm{q}W} \frac{dC}{d\omega} \frac{\omega}{\mathrm{k}T} \tag{3.14}$$

Equation 3.14 allows determination of the defect density from the differential of capacitance with respect to ω. This does however assume linear band bending, which is the biggest source of inaccuracy. Improved accuracy is possible through parabolic band models which are particularly useful for $np+$ junctions [19].

Other reports in literature of TAS in polycrystalline thin film PV devices have used the equation 3.11 in the form;

$$\omega_0 = 2N_V v_{th}\sigma_A \exp\left(-\frac{E_A}{\mathrm{k}T}\right) = 2\xi_0 T^2\left(-\frac{E_A}{\mathrm{k}T}\right) \tag{3.15}$$

where E_A is the activation energy of the defect [21–23]. Here the 'thermal emission pre-factor' $\xi_0 = \nu_0/T^2$ [19], where the value ν_0 ('attempt-to-escape frequency') is equal to $\beta_p N_V$ (the $\sim T^2$ dependence of ν_0 arises from the temperature dependence ($T^{1/2}$) of the thermal velocity v_{th} which affects β_p, and the $T^{3/2}$ temperature dependence of N_V). The emission pre-factor ξ_0 is proportional to the capture cross section, σ_A, and is the temperature independent part of the product $v_{th}N_V\sigma_A$. The capture cross section is assumed to be constant, with no temperature dependency [23]. When 3.15 is rearranged it provides a method for determining ξ_0 and E_A from an Arrhenius-like plot as shown below.

$$ln\left(\frac{\omega}{T^2}\right) = ln\Big(2\xi_0\Big) - \frac{E_A}{\mathrm{k}T} \tag{3.16}$$

Identifying ξ_0 allows calculation of σ_A as follows:

$$\sigma_A = \frac{2\xi_0 \mathrm{h}^3}{16\pi g \mathrm{k}^2 m_{dh}} \tag{3.17}$$

where h is Planck's constant, g is the degeneracy factor and m_{dh} is the effective mass of the holes [24, 25].

When the value of ξ_0 has been calculated, it can be used to determine an energy scale as below;

$$E_\omega = E_A(\omega) = \mathrm{k}T ln\left(\frac{2T^2\xi_0}{\omega}\right) \tag{3.18}$$

This scale can be used as the x-axis for the trap density equation (3.14): when curves are plotted for temperatures in which a capacitative dispersion was observed, their peaks overlap at the value of E_A, with the peak height at the value of N_t.

As has been touched upon here, unlike deep level transient spectroscopy (DLTS), TAS only samples traps near the Fermi level, and is only able to detect majority carrier traps. The obtained values for E_A and σ_A are not likely to be as accurate as those obtained through DLTS. Partly this is through the interaction between deep and shallow states, and partly through the assumption of a T^2 dependence of ν_0. In reality there is often a slightly different temperature dependency, and the measured values differ slightly from the actual energy values. As such, the calculated activation energy, trap density and capture cross section in TAS are all termed 'apparent', and given the symbols E_{nA}, N_{nt} and σ_{nA} in this thesis. Although the precise values are not possible with TAS, the

apparent values measured can be used to define a trap signature, the behaviour of which can then be observed as a function of device processing [9].

3.3.4 Equivalent circuit analysis

In the 1960's Sah suggested that individual traps could be modelled by a series of capacitors and resistors [26, 27]. Indeed, the behaviour of any electrical device can be explored by attempting to approximate it through the use of capacitors, inductors, resistors and distributed circuit elements. This can sometimes reveal valuable information about the device which is otherwise difficult to detect. A bulk resistance may be estimated by a single resistance, and regions of space charge polarisations might be represented as a capacitance. There are some simplifications made in this process however. Simulated circuit elements are ideal, with constant behaviours. In reality a resistor, for example, has a distribution in space and will demonstrate small inductive and capacitive effects along with a response time delay [18]. Another distributed component that is commonly used in equivalent circuits is a constant-phase element (CPE). This describes an imperfect capacitor, with inhomogenous surfaces. The impedance of a CPE is defined by two values as in the equation below:

$$Z_{CPE} = \frac{1}{CPE_T(i\omega)^{(CPE^P)}} \tag{3.19}$$

The exponent value CPE^P can range between 0 (where the CPE acts as a resistor) and 1 (where the CPE acts as a capacitor). The use of a CPE in equivalent circuit analysis allows a good fit to data in the presence of a physical and energetic distribution of charges within a device.

FRA data that is collected for TAS and $C-V$ profiling is similar to that required for equivalent analysis, namely Z' and Z'' (the real and imaginary components of Z) over a range of frequencies. The device can also be studied under DC bias to observe different junctions in a device. Combinations of circuit elements describing equivalent electrical models of devices have elsewhere been used to explore characteristics and junctions, providing useful insights into complex systems [28–31].

3.4 References

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4. Experimental details

This chapter gives details of the experimental practice used in this work. Section 4.1 describes the layer growth, processing and device fabrication, with the experimental details of electrical characterisation detailed in section 4.3. The description of the general methods are presented here while specific details of individual sample series is deferred until the appropriate results chapters. The sample characterisation experiments were:

1. Illuminated $J-V$ performance measurements (room temperature)
2. External quantum efficiency (room temperature)
3. Frequency response analysis (temperature cycle over range 110 - 310 K)
4. Capacitance voltage analysis (300 K)
5. Current-voltage-temperature measurements (temperature cycle over range 200 - 300 K)

During the preparatory experiments for this thesis it was noted that the samples could become damaged during thermal cycling, so this experimental order was chosen to obtain results in order of decreasing importance.

4.1 Film growth and device fabrication

All glass used was coated with SnO_2:F supplied by NSG, with sheet resistances as specified in the results chapters. When used, ZnO buffer layers were deposited at room temperature. CdS and CdS:O layers were deposited by sputtering at 200 °C. CdTe layers were grown through close space sublimation under a nitrogen atmosphere at 25 Torr with the source at 605 °C and the sample at 520 °C. The back surface was etched with nitric/phosphoric (NP) etch in the ratio 70:29:1 H_3PO_4:H_2O:HNO_3 as specified in the individual methods. Nine identical gold contacts were applied by evaporation.

4.2 Description of samples

For the growth of the sputtered CdS layer a (5 x 5) cm square of TCO-plated glass was used as the substrate. During the CSS deposition, the sample was rotated. The thickness of CdS varied slightly across the glass, with a thicker layer at the centre, becoming thinner radially outwards. This is represented in figure 4.1 with darker material towards the centre of the sample.

In order to fit within the CSS chamber, each (5 x 5)cm square was broken into four (2.5 x 2.5)cm squares for growth of the CdTe layer. An array of nine gold contacts was then applied to this. Post-growth processing such as thermal annealing or annealing in the presence of chlorides was then undertaken as specified for each study. For all the cells analysed throughout this work the back contact size was 0.24 cm^2. As the sheet resistance of CdTe is very high (in the order of k$\Omega/\square$ or greater[1]) the lateral conduction is diminished and each device is independent. This 3 x 3 array of contact dots is referred to as a 'sample plate'. Most of the

[1]Sheet resistance is determined using a four-point probe technique, and represents a special 'square' geometry, which is commonly given the unit of $\Omega/\square$. This is dimensionally the same as Ohms, but is specifically used for sheet resistance.

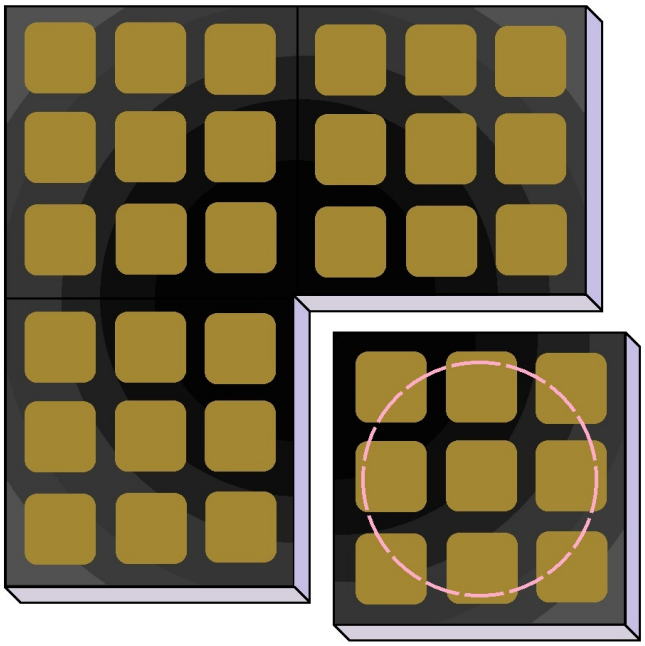

Figure 4.1: Diagram showing the fabrication of CdTe solar cell contact squares starting with a (5 x 5) cm glass square. First the CdS or CdS:O window layer is sputtered onto the whole glass plate (rotation ensures minimum non-uniformity). The sample is quartered into (2.5 x 2.5) cm pieces for deposition of the CdTe by CSS - this deposition is non-uniform and the thicker central region is indicated by the dotted circle. Nine gold contact dots are applied to each quarter to complete the device.

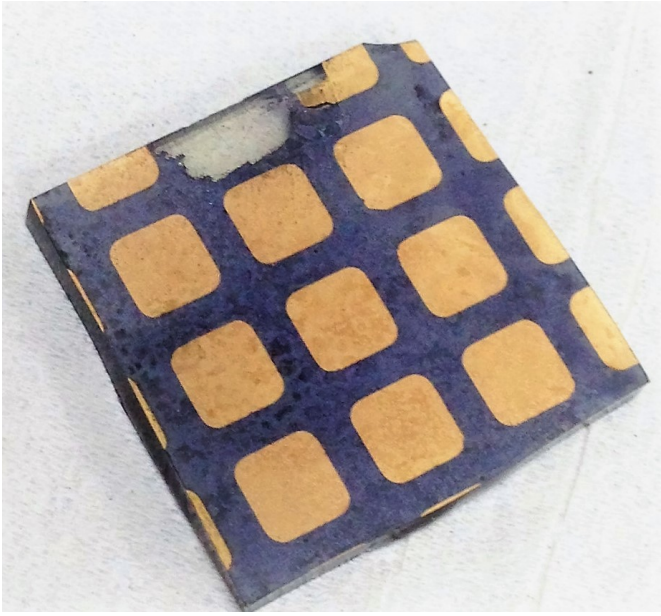

Figure 4.2: A ~ (2.5 x 2.5) cm square completed quarter with 9 intact gold contacts acting as 9 separate solar cell devices. Each 'sample plate' in this study refers to one of these (2.5 x 2.5) cm plates.

studies in this work use multiples of four samples, with four originating from the same piece of glass as seen in figure 4.1. Each will have experienced identical growth conditions prior to CdTe deposition, allowing for a direct comparison of the various processing the quarters have been subject to following separation.

An example of a sample plate is shown in figure 4.2. The gold areas visible in Figure 4.2 act as the individual back contact for each cell, and the clear area uppermost on the quarter is exposed TCO which acts as the common front contact for all 9 cells. This area is formed by scraping away the CdTe and contact layer with a sharp tool, then removing the now exposed CdS with dilute HCl acid to expose the TCO underneath. For $J-V-T$ studies, $C-V$ analysis and frequency response analysis, the cells were connected to the measuring equipment by fixing fine copper wire to the contacts using adhesive silver paste. For illuminated performance and EQE studies the contacts were formed through direct connection with flexible metal contacts.

4.3 Characterisation methods

4.3.1 Performance and external quantum efficiency measurements

$J-V$ analysis was performed under AM1.5 spectrum illumination at an intensity of 100 mW cm^{-2}. A TS Space Systems solar simulator with a metal halide arc lamp was the illumination source. Electrical measurements were taken using a LabVIEW controlled mechanical jig designed and built by Dr. L. Phillips, which moved the sample to ensure identical illumination conditions for all contact dots on each sample plate. A Keithley 2400 Source Monitor was used to measure the current at supplied voltages every 0.05 V between -1 to 1 V.

External quantum efficiency (EQE) measurements were taken using a Bentham PVE300 system without light bias. Readings were taken at every 5 nm between 300 - 900 nm, with three repeat readings for each tested contact dot.

4.3.2 Temperature dependent current-voltage measurements

4.3.2.1 Dark measurements

Temperature dependent current-voltage ($J-V-T$) measurements were conducted under vacuum in the light and the dark. The equipment comprised a CTI-Cryogenics refrigerator, with a CTI-Cryogenics 8200 compressor and a Lakeshore 331 Temperature Controller. The cryostat was manufactured by Janis Research Co. The electrical measurements were taken using a Keithley 2400 Source Monitor and an automated LabVIEW program as designed by Dr. L. Phillips. $J-V$ readings were taken at 10 K intervals from 300 - 200 K with a 10 minutes of temperature stability before a reading was taken. Three readings were taken at each temperature, but only one temperature cycle was performed.

4.3.2.2 Light measurements

For illuminated $J-V-T$ studies as shown in chapter 6, the basic equipment was used as for dark measurements. In addition, an Oriel solar simulator with AM1.5 filters was used to project light onto the front of the contact dot under test through a window in the cryostat. The optical system was adjusted with a system of mirrors and lenses so the output J_{SC} of the test device matched

with that taken previously under the TS Space Systems simulator. For studies under varied illumination, neutral density (ND) filters were used to control the light intensity. $J-V-T$ readings were taken at 10 K intervals from 200 - 300 K at illuminations of 0, 1, 13, 25, 40, 63 and 100% of ~AM1.5 spectrum.

Illuminated capacitance voltage ($C-V$) measurements were taken using a Ametek Solartron Analytical Modulab XM 1260 Impedance/Gain Phase Analyser equipped with a 1296 Dielectric Interface. The same experimental technique was used as for dark measurements in section 4.3.3.

4.3.3 Capacitance-voltage measurements

Capacitance-voltage ($C-V$) measurements were taken in the dark under vacuum at 300 K. The equipment comprised a CTI-Cryogenics refrigerator, with a CTI-Cryogenics 8200 compressor and a Lakeshore 331 Temperature Controller. The cryostat was manufactured by Janis Research Co. Electrical measurements were taken with a Solartron SI 1260 Impedence/Gain Phase Analyser with a 1296 Dielectric Interface.

The DC bias level was swept from -1 to 1 V with readings taken at every 0.05 V. Using a ripple voltage of 25 mV the voltage frequency was swept between 1 Hz - 1 MHz, with measurements of impedance at 25 points per decade (logarithmically spaced).

The data recorded at each point were as follows:

Parameter	**Symbol**	**Units**
AC and DC voltages	V	V
Frequency	f	Hz
Temperature	T	K
Impedance (Real)	Z'	Ω
Impedance (Imaginary)	Z''	Ω
Admittance	G	S
Capacitance	C	F

Table 4.1: The data collected during $C-V$ and FRA analysis.

The data was analysed at 0.1 MHz unless otherwise stated.

4.3.4 Frequency response analysis (FRA)

4.3.4.1 AC measurements

AC frequency response analysis (FRA) measurements were taken in the dark under vacuum. The equipment used was identical to that used for $C-V$ measurements, namely a CTI-Cryogenics refrigerator, with a CTI-Cryogenics 8200 compressor, a Lakeshore 331 Temperature Controller and a cryostat manufactured by Janis Research Co. Electrical measurements where taken with a Solartron SI 1260 Impedence/Gain Phase Analyser with a 1296 Dielectric Interface.

The temperature was cycled from 290 - 110 K, then 110 - 310 K, then 310 - 290 K. Readings were taken at every 10 K on every part of the cycle to produce two readings for each tested temperature. The bias was set (for devices in chapters 6 and 7 a 0 V bias was used, for chapter 5 samples the DC bias was varied from -0.3 to 0.9 V, with frequency response data taken at every 0.3 V). A ripple voltage of 25 mV was used with a frequency that varied from 1 Hz - 1 MHz, with measurements of impedance taken at 20 points per decade (logarithmically spaced). The data recorded was as for $C-V$ analysis.

This data was used in two ways:

a) using the thermal admittance spectroscopy methodology as described in section 4.3.4.2

b) to allow inference of the equivalent circuit for the device as described in section 4.3.4.3

4.3.4.2 Interpretation of FRA data using thermal admittance spectroscopy methodology

Thermal admittance spectroscopy is a commonly used technique for observing majority trap behaviours. There are several excellent papers and books with guidance on the technique (see section 3.3.3 for references), but it can be difficult to find a definitive source.

The methodology used in this work is described here as a detailed procedure, and a worked example is shown in Appendix A. Rearranging large numbers of data prior to performing calculations can be tiresome and prone to error. If a significant number of samples are to be examined, it is highly recommended to make a template which will rearrange and perform the calculations automatically from the raw data.

The steps involved in practical data gathering and analysis are:

1. Collect FRA data as described above.

2. Import raw data into data analysis and graphing software of choice (OriginPro used for this work).

3. For the data collected here, as there were two readings taken at each temperature (taken at different parts of the cycle) the plots of C vs f of both values (at 120, 200, 290 and 310 K) were compared to ensure the data had not deviated with time. The data for matching temperatures were then averaged.

4. With a spreadsheet as a function of frequency, f, create columns for $ln\, f$ and $\omega = 2\pi f$.

5. For each averaged temperature data, as a minimum, calculate the following two parameters (where G_D is the conductance value at ~DC voltage) and plot each parameter separately as a function of frequency on a log/log graph (with all T on one graph);

$$\text{Reduced conductance} = \frac{G - G_D}{\omega} \qquad \text{Differential capacitance} = f\frac{dC}{df}$$

6. It is also useful to calculate and graph the following to observe appropriate behaviours (although it is not required for calculations);

$$Z' \text{ vs } -Z" \qquad log(f) \text{ vs } -\theta \qquad log(f) \text{ vs } C \qquad log(f) \text{ vs } G$$

7. On the plots of reduced conductance and differential capacitance, look for peaks that move with temperature, they are unlikely to be visible at every temperature. There may also be more than one in each temperature's curve, visible at different frequencies. Some peaks may be visible in one parameter but not the other.

8. Fit these peaks and record the peak's frequency position at each visible temperature.

9. Plot these peak positions on an Arrhenius plot of $ln(\omega/T^2)$ vs $1/T$ according to equation 3.16.

10. From a linear fit of the Arrhenius plot (and the use of equation 3.16), calculate ξ and E_{nA} from the intercept and slope respectively. For peaks visible in both reduced conductance and differential capacitance, the linear fits should produce similar results.

11. Use the value of ξ from above to plot trap density N_t as a function of energy E using the following equations (where W is the width of the depletion region);

$$E = \frac{\mathrm{k}T}{\mathrm{q}}\, ln\left(\frac{2T^2\xi}{\omega}\right) \qquad \text{vs} \qquad N_t = \frac{dC}{d(ln\,\omega)}\frac{-\xi}{\mathrm{k}TW}$$

with all temperatures on the same plot.

12. If the value of ξ from the Arrhenius plot is correct, the graph above (for the temperatures used to populate the Arrhenius plot) should demonstrate a peak at the value of E_{nA} calculated in step 10, where the peak height corresponds to the trap density, N_t.

(If peaks are not easily apparent on the plots discussed in step 5 there are alternatives which can be tried, such as $dC/d(ln\,f)$.) A 'placeholder' value of the depletion width $W = 1\,\mu\mathrm{m}$ was used and later a correction made using the value for W calculated separately in $C-V$ analysis.

Some peaks were difficult to separate or fit on the reduced conductance or differential capacitance plots (resulting in very few data points on the Arrhenius plot) but produced a good fit on the E vs N_t plot in step 11. In these cases, to minimise the error on the extracted values, an 'overlap' technique was used. Using the value of ξ extracted from the Arrhenius plot as a starting point (ξ_A), the peak positions on the E vs N_t plot were measured. By increasing and decreasing the the value of ξ, the peaks would move and separate, and their average peak energy position and standard error was recorded as a function of ξ_A. When plotted, a value of E emerged which had the lowest standard error in mean peak position. This was determined to be E_{nA} and the corresponding value of ξ_A taken as a more accurate estimation of ξ.

4.3.4.3 Interpretation of FRA data using equivalent circuit analysis methodology

For any given electrical circuit or material/device that can be probed with FRA methods, it is possible to use the data to infer equivalent circuits that are consistent with the FRA spectra. However, for any electrical system there exist an arbitrary number of equivalent circuits which can fit the experimental data. The most valuable circuits have a physical basis and as such are capable of giving physical insight. In the case of CdS/CdTe solar cells, the work of Proskuryakov [1] reviewed in section 2.3.4.1 describes such a development: firstly it was demonstrated that for cells fabricated from CdTe of different grain sizes, $R-C$ elements

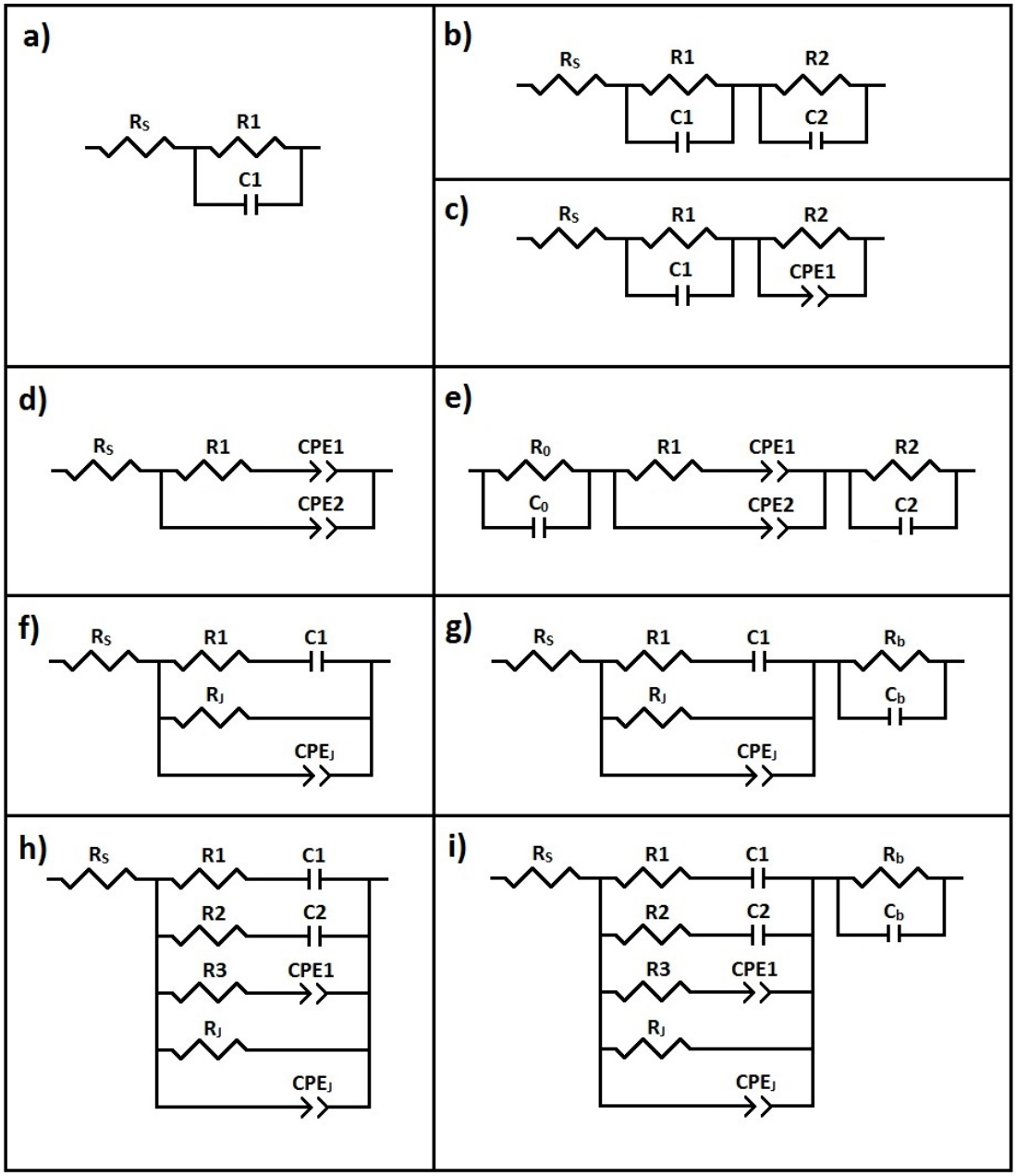

Figure 4.3: The equivalent circuit models (a) to (i) considered in this work. See table 4.2 for description of the components.

could be included in the circuit that account for the electrical behaviour of grain boundaries. Secondly it was shown that the adverse effects of grain boundaries was high for untreated samples, and was reduced following chloride treatment to such an extent that the grain boundary equivalent circuit element was negligible. These two models are shown in figure 4.3 (e) and (d) respectively, and are among the models used in this work.

Further to the models of Proskuryakov, additional equivalent circuits were devised and also tested against experimental data in this work. The devised models are shown in figure 4.3 f) and g). The models increase in complexity from (a)-(i), which also lends credence to their suitability when describing a cell: A model which accurately fits the data using less electrical components is both a) more likely to be a correct representation, and b) more likely to provide useful information about cell behaviours. The justifications for each model and a brief description of cell structure the components represent is shown in table 4.2.

The following methodology was used to fit equivalent circuits using the ZView software package. The software was found to be very useful but had a number of issues to be aware of. There was no restriction of parameter values (other that positive or negative), such that unphysical and unfeasible values were permitted. For example, excellent fits were often possible with CPE^P values $\gg 1$ (the physical range is 0 - 1), or a capacitance in mF or greater. Repeated iterations of fitting could also find different local solutions, so manual oversight and judgement was required to direct the software to a probable solution.

- The raw impedance data for Z' and Z" collected in section 4.3.4.1 needed to be formatted in a particular way in order to be read by the ZView.
- The circuit designs shown in 4.3 were added into the software's equivalent circuit library.
- ZView has a number of initial programs which allow quick estimation of some parameters such as R_S, which sometimes proved useful where fits were difficult.
- The data was analysed over a restricted frequency of 10 - 10^5 Hz, as above the upper limit the data was found to be anomalously affected by the back contact, and many fits were not possible if this data was included.
- The same frequency range was used for all samples, as the 'goodness of fit' measure, (in ZView named the 'sum of the squares', here referred to as R^2) is dependent on the number of data points.

Model	Description	Reference
a	Single diode model with the cell series resistance represented by R_S	[2]
b	Double diode model, with a series resistance R_S	
c	As model (b), with a substitution of CPE_1 for C_2 to represent non-uniform capacitance of the $p-n$ junction.	[3]
d	A circuit found by Proskuryakov *et al* to describe etched CdS/CdTe cells, where CPE_1 represents non-uniform capacitance of the $p-n$ junction and CPE_2R_1 represents the $p-n$ junction's non-uniform resistance.	[1]
e	The same circuit as in (d) with the addition of a parallel R_2C_2 section, which was thought to represent grain boundaries in unetched samples. There is also an additional capacitor C_0, which, in conjunction with the parallel R_0, describes the back contact.	[1]
f	A simplified version of model (h) with only one trap level (R_1C_1) represented.	
g	In a similar manner to (f), this is a simplified version of model (i) with only one trap level (R_1C_1) represented.	
h	A non-ideal diode with several trap levels, represented by $C_i - R_i$ pairs ($i = 1 - 3$). The main junction elements are represented by C_J and R_J	[2]
i	The same electrical structure as in model (h) but with the back contact simulated with a parallel R_B and C_B section.	[2]

Table 4.2: The rationale behind the different equivalent circuits (a) - (i) from figure 4.3 considered in this work.

- For the comparatively simple circuits 'a'-'d' all parameters were left free initially, which often lead to good solution. Occasionally one segment would be fixed while other segments fitted, before becoming free parameters again.

- For the more complicated circuits 'e'- 'i' this approach was not feasible. The fit component would be initially given approximate values using ZView's quick estimation parameters, before fitting of components in a stepwise fashion. Resistance or parallel RC segments were fitted first, before gradu-

ally making other series components free parameters, and fitting the CPE^P values last.

- For some fits, ZView could not find a local solution, and would return component values of zero. This occurred more frequently in fitting of complex circuits such as 'h' and 'i'. These circuits were also found to progress towards a number of different solutions depending on the initial values the components were given.

In some cases, if a local solution was not forthcoming, the initial values would be seeded with those from a similar device, or different voltage, or different circuit model. Occasionally this led to feasible solutions which had not been apparent before.

4.4 References

[1] J. D. Major, Y. Y. Proskuryakov, and K. Durose, "Impact of CdTe surface composition on doping and device performance in close space sublimation deposited CdTe solar cells," *Progress in Photovoltaics: Research and Applications*, vol. 21, no. 4, pp. 436–443, 2013.

[2] Y. Y. Proskuryakov, K. Durose, B. M. Taele, and S. Oelting, "Impedance spectroscopy of unetched CdTe/CdS solar cells - equivalent circuit analysis," *Journal of Applied Physics*, vol. 102, no. 2, p. 024504, 2007.

[3] Y. Y. Proskuryakov, K. Durose, M. K. Al Turkestani, I. Mora-Seró, G. Garcia-Belmonte, F. Fabregat-Santiago, J. Bisquert, V. Barrioz, D. Lamb, S. J. C. Irvine, and E. W. Jones, "Impedance spectroscopy of thin-film CdTe/CdS solar cells under varied illumination," *Journal of Applied Physics*, vol. 106, no. 4, p. 044507, 2009.

5. Effects of varying the $MgCl_2$ treatment time on CdTe solar cells

5.1 Introduction

This chapter presents a systematic study of the influence of activation of CdTe solar cells with magnesium chloride on their performance and underlying device and materials properties. These include contact barrier height, trap parameters, doping profile, transport mechanism and equivalent circuits. As discussed in chapter 1, despite many years of research into chloride activation there is as yet no definitive consensus on the mechanism of the activation, and even on some of the above parameters. In order to maximise the efficacy of the activation step, the effects of this chemical processing must be fully understood. To this end the current chapter describes experiments conducted on cells where the activation time is varied, and the analysis of the ensuing changes in cell behaviour and parameters.

There are two experimental series described in this chapter, each of which has a different window buffer layer as shown in table 5.1. Series 521 (CdS buffer layers)

Study	**Series 521**	**Series 522**
Window layer	CdS	CdS:O
Anneal time variation	Yes	Yes
Varied anneal temperatures	No	Yes
Anneal without Cl	No	No

Table 5.1: The two sample series explored in this chapter, both of which were processed with $MgCl_2$ for varying times. Series 521 has a CdS window layer (as described in section 5.2.1) and Series 522 has a CdS:O window layer (see section 5.2.2).

demonstrated some systematic variation in trap behaviour. This was followed by Series 522 (CdS:O buffer layers), and although the expected validation of the data set from a larger sample size did not emerge as clearly as expected, some comparison could still be drawn as described in section 5.4.

5.2 Description of samples examined in this chapter

5.2.1 CdTe cells with CdS window layer having varied $MgCl_2$ treatment times (Series 521)

This study comprised eight sample plates of identically grown cells post-growth processed with aqueous $MgCl_2$ then annealed for a range of times. The cells were grown in-house by Dr. J. D. Major. TEC7 soda-lime glass supplied by NSG (coated with SnO_2:F) was used as the substrate. RF sputtering in argon was used to deposit a 100 nm ZnO layer and a 120 nm CdS layer, followed by a ~4 µm CdTe layer deposited by CSS. Following etching for 15 s in nitric/phosphoric (NP) acid mixture the samples were sprayed with 1 M aqueous $MgCl_2$ and annealed in air in a tube furnace at 410 °C for a range of time periods between 0 and 50 minutes. A further 15 s etch in NP acid preceded application of evaporated gold contacts.

5.2.2 CdTe cells with CdS:O window layer having varied $MgCl_2$ treatment times (Series 522)

Similar to the first set in design, this series examined twelve sample plates subjected to different anneal times after aqueous chloride application, but in contrast the window layer was CdS:O. They were also manufactured by Dr. J. D. Major. TEC7 soda lime glass was used as the substrate, with a 100 nm ZnO layer and a 120 nm CdS layer grown through RF sputtering in an argon atmosphere with 7% O_2. A ~4 µm CdTe layer was then deposited by CSS and etched with NP acid for 15 s. A 1 M aqueous $MgCl_2$ solution was applied before air annealing in a tube furnace. For nine plates the annealing temperature was 410 °C for times of 10 - 60 minutes. Three plates were annealed at 390 °C for 30 - 50 minutes. As before a second 15 s NP etch was performed before the gold contacts were evaporated on to the samples.

5.3 Results

5.3.1 CdTe cells with CdS window layer having varied $MgCl_2$ treatment times (Series 521)

5.3.1.1 Performance data

a) Efficiency and working parameters

The performance of the cells under AM1.5 illumination is shown in figure 5.1. Each plate has up to 9 cells (contact dots) but short-circuited cells were not included in the analysis. It can be seen that for all four performance parameters there appears to be a local maximum in performance after chloride annealing for 25 minutes (the 50 minute sample (521/8) is slightly anomalous, but the number of unshunted devices was unusually low).

Figure 5.2 shows a comparison of the $J-V$ curves from the best performing

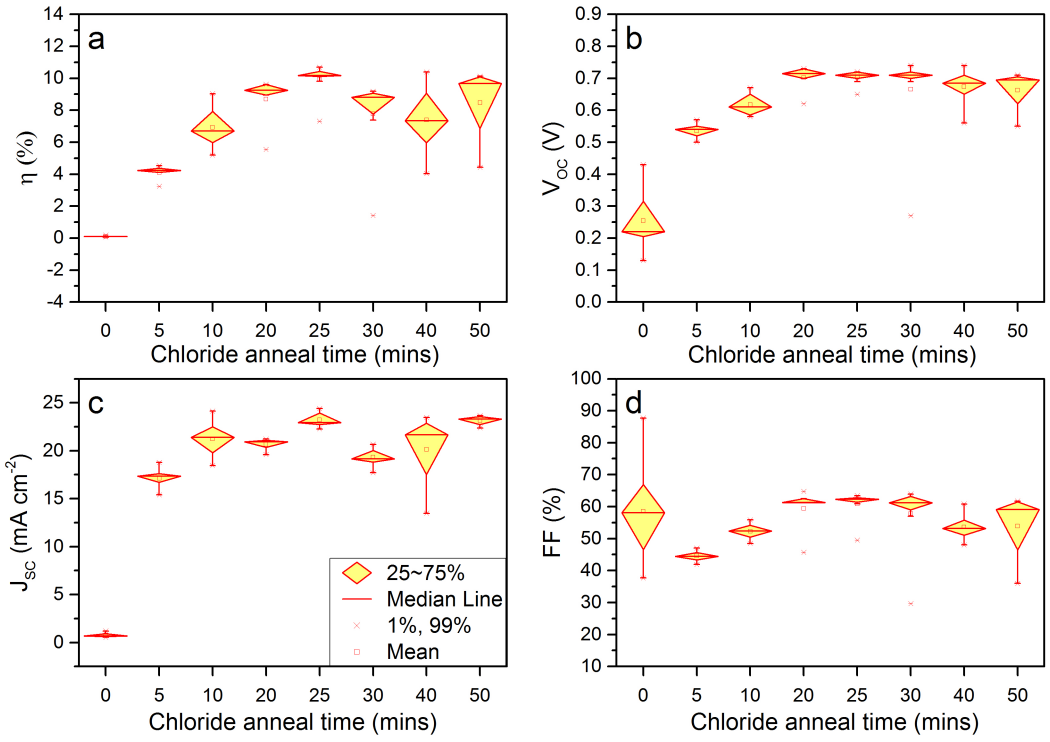

Figure 5.1: Box plots demonstrating the spread of performance data for N contact dots (max $N = 9$) for CdS/CdTe devices as a function of chloride treatment time (Series 521), showing a) efficiency η, b) open circuit voltage V_{OC}, c) short circuit current density J_{SC}, and d) fill factor FF. The coloured trapezoid contains the inner 50% of data points, with the median and mean values being marked with a line and a box consecutively. See section 5.3.1.1 for discussion.

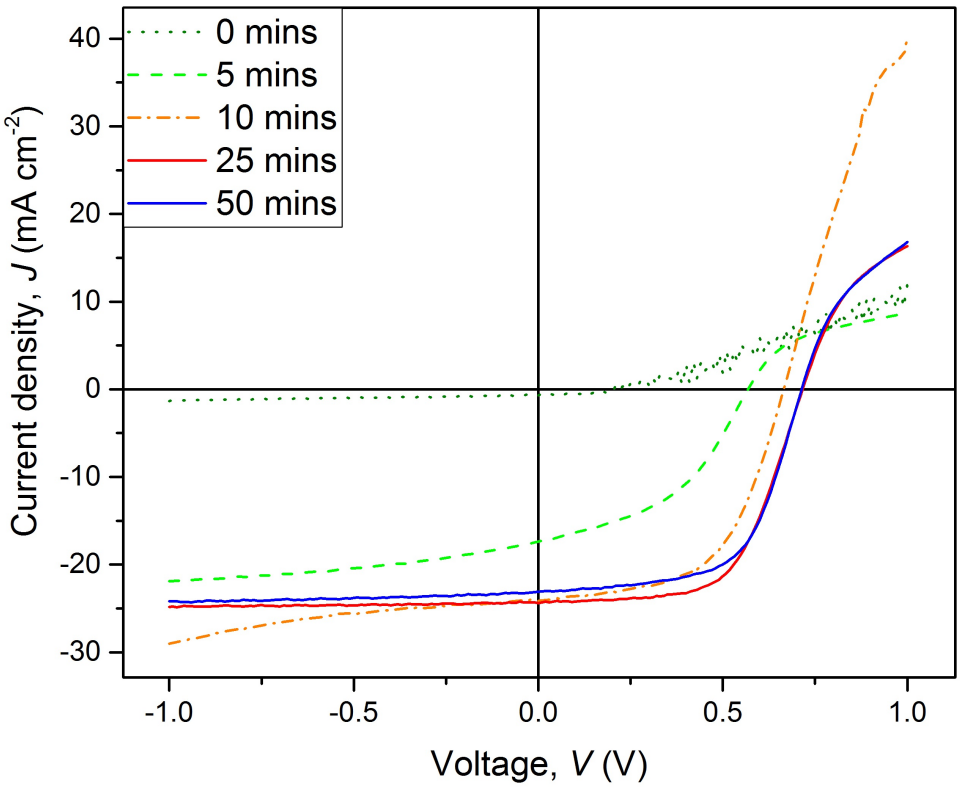

Figure 5.2: $J-V$ curves of the best performing cells for chloride treatment times of 0, 5, 10, 25 and 50 minutes. See also figure 5.1.

cells for each processing time. There is a systematic development of the curves. The as-grown device has only weak diode behaviour but treatment for just 5 minutes caused rectification. Treatment for 10 minutes caused the J_{SC} to reach its plateau value of $\sim 24\,\mathrm{mA\,cm^{-2}}$ while continued treatment to 25 minutes caused V_{OC} to continue to improve to its maximum of $\sim 0.70\,\mathrm{V}$. Further processing to 50 minutes caused the onset of a decline in overall performance. Examination of the curves in figure 5.2 revealed other trends. From the slope of the $J-V$ curve in reverse bias it can be seen that full chloride treatment ($\geq$ 25 minutes) reduced the series resistance (typically from $> 300\,\Omega\,\mathrm{cm^{-2}}$ to $< 100\,\Omega\,\mathrm{cm^{-2}}$). For all of the devices there were varying degrees of forward bias current limitation or 'roll over' and this is widely considered to be due to the non-Ohmic back contact behaviour.

b) EQE

External quantum efficiencies of typical cells are compared in figure 5.3. The as-grown sample demonstrated almost no photo-activity, but a slight peak at longer wavelengths indicates a buried homo-junction [1], i.e. the electrical junction is deep in the CdTe and is only reached by highly penetrating low energy photons. Again it evident that within the first few minutes of chloride activation a dramatic

change has occurred. The 5 minute curve already displays the expected features of a heterojunction (p-CdTe/n-CdS) cell, including the CdS absorption cut-off at ~500 nm/2.5 eV.

The EQE data for the 5 to 50 minute plates in figure 5.3 demonstrated several features that are common to all curves. The step changes across the wavelength range are the results of separate processes, which are as follows, in order of increasing wavelength:

i. The short wavelength cut-off at ~380 nm, due to absorption in the transparent conductor,

ii. The window layer absorption between 380 nm - 500 nm, bounded by the band-gap of the CdS,

iii. The long wavelength cut-off at ~850 nm/1.5 eV due to the band gap of the absorber layer,

iv. The contribution from 550 - 850 nm is peaked towards lower wavelengths, indicating the electrical junction position is close to the CdS/CdTe interface.

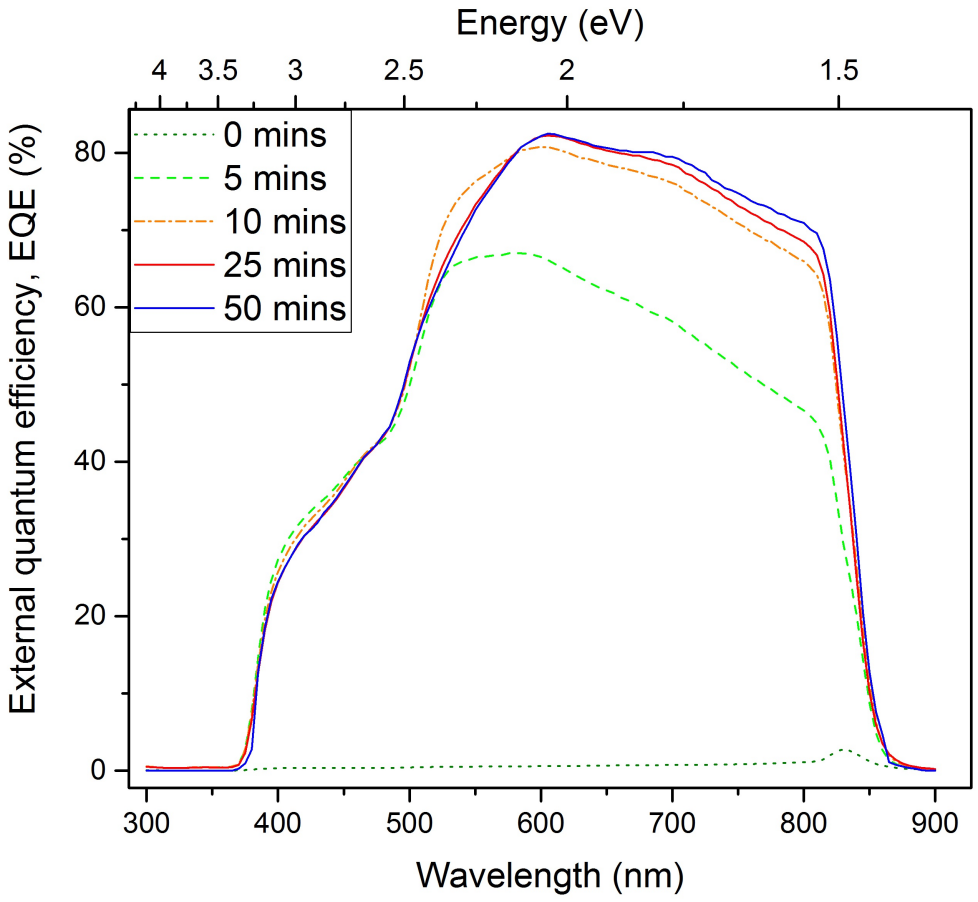

Figure 5.3: EQE curves of typical CdS/CdTe cells for chloride treatment times of 0, 5, 10, 25 and 50 minutes from Series 521. See also figures 5.1 and 5.2.

After 5 minutes the absorption increased significantly (corresponding to an increasing J_{SC}), but after 10 minutes this plateaued. This is consistent with the $J-V$ data. The small differences between the 10 and 25 minute samples at 500 nm are likely to be related to alloying of CdS and CdTe at the interface creating $CdS_{1-x}Te_x$.

5.3.1.2 Current transport

a) Main junction

The current transport was examined through $J-V-T$ studies as described in section 3.2.3. The data for Series 521 is shown in figure 5.4. Panels a - c show the evolution of $ln\,J$ vs V as a function of T for samples that are a) under-treated (5 minutes), b) optimised (25 minutes), and c) over-treated (50 minutes). The differences in the three kinds of behaviour imply changes in current transport, and these changes are now described and discussed in terms of the reverse bias saturation current (J_0), slope (A), and diode factor (n) behaviours.

In forward bias up to a voltage of ~ 0.6 V the $J-V-T$ curves were analysed for an appropriate fit to current transport models as discussed in section 2.2.3. For multi-step tunnelling the forward current, J_f, should obey the following equation;

$$J_f = J_0\, exp(AV) \tag{2.12}$$

where

$$J_0 = J_{00}\, exp(BT) \tag{2.13}$$

Equation 2.13 implies that in this model there should be a positive, linear relationship between $ln\,J_0$ and T.

Values of J_0 were extracted from the data as explained in Appendix B. The graphs for $ln\,J_0$ vs T are shown in figure 5.4 d). Each curve represents a different $MgCl_2$ treatment time in the range 0 - 50 minutes. The 5 minute sample had a relatively large value of $J_0 \approx 4 \times 10^{-4}$ mA cm^{-2} ($ln\,J_0 \approx -15$) at 200 K , which demonstrated a slight increase with rising temperatures. With the exception of the 25 minute sample, all the other samples displayed a similar trend - a decreasing or invariant $ln\,J_0$ with increasing T below 250 K and an almost linear increase with T above 250 K. The room temperature values for $ln\,J_0$ decreased as a function of $MgCl_2$ treatment time to the lowest value of $J_0 \approx 2.5 \times 10^{-7}$ mA cm^{-2} ($ln\,J_0 \approx -22$) in the 30 minute sample before increasing in magnitude again. The behaviour of the 25 minute sample was somewhat different - there was an invariance of $ln\,J_0$ with T temperatures below ~ 250 K, whereas the value of $ln\,J_0$ decreased above this temperature.

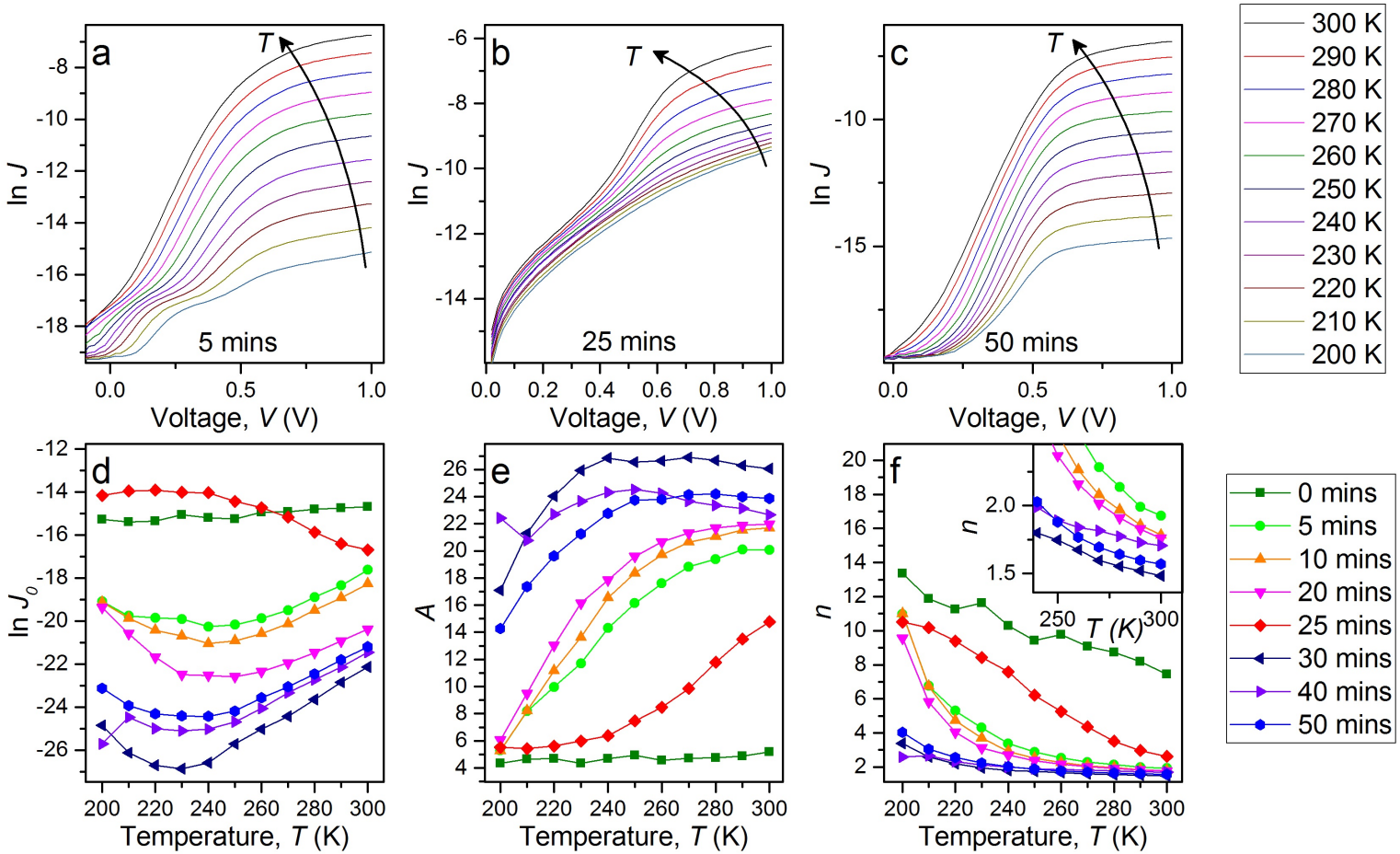

Figure 5.4: Data from $J-V-T$ studies on Series 521. The upper set of plots demonstrate the three major observed trends, and show $ln\, J$ for samples a) 521/2 (5 mins), b) 521/5 (25 mins) and c) 515/8 (50 mins). The lower row contains data from all eight sample cells from Series 521, and plot temperature behaviour of d) $ln\, J_0$, e) A and f) n. The corresponding legend is on the same row as the plot.

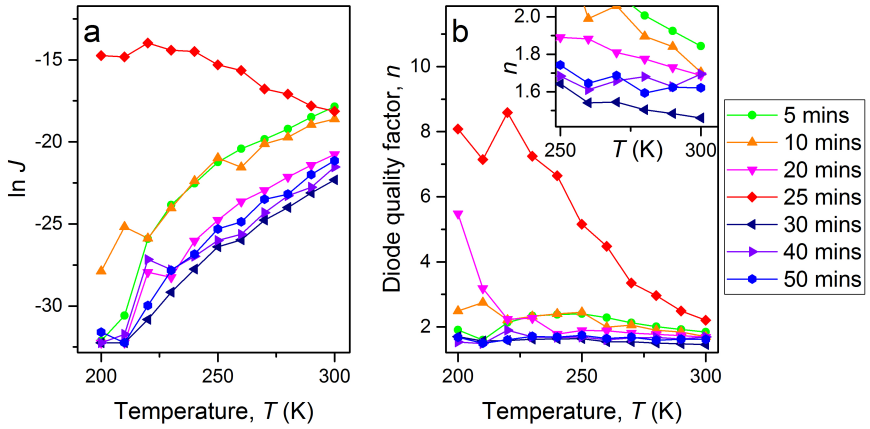

Figure 5.5: Parameters calculated for Series 521/2 - 8 (5 - 50 mins) using the single diode model; a) $ln\, J_0$ as calculated for Series 521/2 - 8 (5 - 50 mins), and b) n vs T, with a closer view in the inset.

An increase in $ln\, J_0$ with decreasing T is anomalous, as reverse current is a thermally activated mechanism in these devices. The presence of this feature in all the sample plates below $\sim$250 K was evidence that the above model does not adequately describe the data below this temperature. A second method was used to extract parameters from the experimental $J-V$ curves: it was to proceed by fitting the curve to the single junction diode equation (equation 3.4) and using the parameters J_0, n, R_S, and R_{SH} as fitting parameters. Details of the method are provided in Appendix B with examples. Briefly, since the equation is transcendental (J appears on both sides) the diode equation was solved by an iterative method using a function in the 'OriginPro' software (Orthogonal Distance Regression [ODR]). Typically for each segment of a $J-V$ curve, solutions were generated in 2 $\sim$5 minutes, but the procedure required manual oversight. Hence for each cell taken in turn, each experimental $J-V$ curve generated the parameters J_0, R_S, and n. Repeating this allows the temperature dependence of the parameters to be established as shown in figure 5.5. On comparing the low temperature curves seen in figure 5.4 d) and 5.5 a), it can be seen that the anomalous current behaviour was not replicated in the values extracted from the single diode model, except in the 25 minute sample. However, above 250 K, the behaviour of both current and diode factor n are comparable between the two models (figures 5.4 f) and 5.5 b). Values of $1 < n < 2$ are acceptable, but $n > 2$ has no physical meaning. Values $n > 2$ are regularly seen in CdTe cells, indicating that these models are not always appropriate for this complex material. Consequently, values for parameters extracted from fitting to equation 2.12 were not analysed for temperatures below 250 K.

Figure 5.4 e) shows the variation of A with temperature. It can be seen

that there was a change in behaviour as a function of chloride treatment time. The as-grown sample (i.e. 0 minutes treatment time) showed a relatively low value of A (<5) which was invariant with temperature. However treatment for just 5 minutes had a profound effect: for this sample A is low at low T ($\sim$5) and rose steadily with increasing temperature to $\sim$18 at 260 K, after which the value became less strongly dependent on T. The 10 and 20 minute samples displayed similar behaviour, with A again tending towards a steady state at higher temperatures. For treatment times of 30, 40 and 50 minutes, A is >14 at 200 K and rises with increasing temperature, until becoming invariant with T after $\sim$250 K. The 30 minute sample demonstrated the highest values of A at room temperature of the samples in Series 521. (The 25 minute sample had markedly different behaviour in keeping with its anomalous behaviour for its $ln\, J_0$ vs T plot: this sample also demonstrated low A at low T but A only began to become temperature dependent at $\sim$250 K, and then increased almost linearly with T up to $\sim$15 at 300 K.)

As discussed previously, the values of A below 250 K are unreliable, as the model has provided unphysical behaviour of $ln\, J_0$. As a consequence only values above 250 K were used in determining the transport processes. For all samples except 521/5 (25 minutes), A becomes invariant with temperature towards 300 K. This is a good indicator of the multi-step tunnelling process. Despite the parameter n having no physical meaning in the multi-step tunnelling model, its behaviour with changing T can be used as an indicator - it is expected to reduce with increasing temperatures, and is not expected to be pinned at a particular level. This is the pattern seen for all samples in figure 5.4 f), where n is seen to decrease with T. This trend is also confirmed on analysis of the same $J-V-T$ data using the single diode equation as seen in figure 5.5 b).

If the multi-step model is correct at room temperature, and equation 2.12 valid, the values of A can be used to calculate the number of tunnelling steps, R, using the method described in section 2.2.3 and the equations below.

$$A = \alpha R^{-\frac{1}{2}} K \tag{2.14}$$

and

$$\alpha = \left(\frac{\pi^2}{2h}\right)\left(\frac{\varepsilon_p m_n}{N_A}\right)^{\frac{1}{2}} \tag{2.15}$$

The results of this analysis are shown in table 5.2. For the calculation of R, the number of uncompensated acceptors, $N_{nA} = N_A - N_D$ was determined by $C-V$ measurements as described in section 5.3.1.3. The number of tunnelling steps R appears to be in the order of hundreds of thousands for the 0 minute

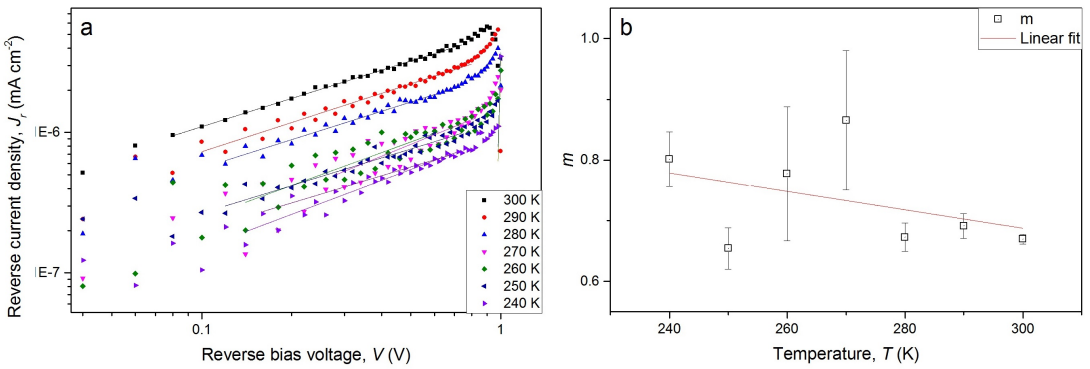

Figure 5.6: Calculation of the gradient of the reverse bias $J-V$ log-log curve, m, for sample 515/6 (30 mins) from a) the $J-V-T$ reverse bias data, and b) plotting the resulting m vs T. A negative gradient is indicative of multi-step tunnelling.

sample, which then reduced by two orders of magnitude by 5 minutes, reaching a minimum at 10 minutes before rising again. The smallest values for R seen were are all one to two orders of magnitude larger than others reported in similar material ($\sim$30 [2], 40 - 50 [3], $\sim$300 [4], 40 - 70 [5]). The quoted studies find similar values for A, but estimate N_{nA} to be one to two orders of magnitude larger ($3.2 \times 10^{16}\,\mathrm{cm}^{-3}$ [2], $3.5 \times 10^{15}\,\mathrm{cm}^{-3}$ [4], $2.7 \times 10^{16}\,\mathrm{cm}^{-3}$ [5] respectively) which accounts for the different values of R. However as the cells studied in this series were not optimised the determined values appear reasonable.

All Series 521 samples were also studied in reverse bias to look for evidence of transport effects including multi-step tunnelling in this region of the $J-V$ curve. Through these analyses, values for the trap density, N_t, at 300 K, and the slope of the reverse bias log-log $J-V$ curve, m, were calculated using the equations below.

$$ln\frac{J_r}{V} = ln\left(aq^2\frac{N_t}{h}\right) - \gamma\left(V_{bi} - V\right)^{-\frac{1}{2}} \tag{2.17}$$

$$J_r \propto V^m \tag{2.18}$$

A typical example of the analysis is shown in figure 5.6. A value of the slope m which reduces with T is taken to be indicative of multi-step tunnelling in reverse bias. All but one of the samples studied in reverse bias (namely 0, 5, 10, 20, 40 and 50 minutes) demonstrated this trait, indicating that multi-step tunnelling is occurring in these samples. For the 25 minute sample, which did not display any evidence of multi-step tunnelling in the preliminary transport analysis, there was an increase of m with T.

The values of N_t in table 5.2 refer to required trap density required for multi-

step tunnelling. The values are not an indication of the number of traps present in the sample, and as such no comparison can be brought between these values and those obtained through TAS later in this chapter.

Sample	**Chloride anneal time** (mins)	N_{nA} (10^{14} cm^{-3})	**Forward bias**		**Reverse bias**		
			A 300 K	n 300 K	R 300 K	N_t 300 K (cm^{-3})	$\Delta m/\Delta T$ 250-300 K
521/1	0	0.89	5.2	7.5	212,000	4.6×10^{10}	-2.2×10^{-3}
521/2	5	1.87	20.1	1.9	6,740	2.4×10^{6}	-2.2
521/3	10	2.78	21.7	1.8	3,970	1.2×10^{6}	-9.7×10^{-1}
521/4	20	1.80	21.9	1.8	5,900	5.3×10^{7}	-8.6×10^{-2}
521/5	25	2.51	14.8	2.6	NA	NA	1.4×10^{-3}
521/6	30	1.44	26.1	1.5	5,200	4.6×10^{4}	-1.0×10^{-3}
521/7	40	1.18	22.7	1.7	8,390	6.3×10^{9}	-1.2×10^{-2}
521/8	50	1.27	24.6	1.6	6,630	8.6×10^{8}	-3.9×10^{-1}

Table 5.2: The results of analysing $J-V-T$ data for Series 521 using the multi-step tunnelling model. The table includes calculated values of slope, A, diode factor, n, and number of tunnelling steps R, which are all calculated from the forward bias data. The reverse bias $J-V-T$ data was used to calculate the trap density required to permit tunnelling, N_t and the exponent m, which can be used to confirm a finding of multi-step tunnelling in these samples. N_{nA} was calculated from $C-V$ analysis and will be discussed in the next section. Calculated errors for all parameters were in the order of 5%.

It can be seen from table 5.2 that the gradient of m vs T was negative for all the tested samples, acting as confirmation that multi-step tunnelling was the dominant mode of transport for all the cells in Series 521 (other than for sample 521/5 (25 minutes) which was anomalous). For Series 521 it is unclear whether the best performing sample, 521/5 (25 minutes), genuinely had a different dominant transport mechanism to the rest of the series, or if the sample was simply too badly damaged from previous experiments to provide good quality data.

b) Back contact

Values for the back contact barrier height for Series 521 were determined through the methods described in section 3.2.3 using $J-V-T$ data. The series resistance R_S was approximated through the slope method, and also through fitting of the single diode equation. It was found that both techniques produced generally consistent results for the back contact barrier height, although for some samples achieving a physically appropriate single diode fit was challenging (see Appendix

B). The results were analysed using the exponential equation below (equation 3.3) and a linear fit to the third term (equation 5.1) An example of the data and fits can be seen in figure 5.7.

$$R_s = R_{\Omega 0} + \frac{\partial R_{\Omega 0}}{\partial T} + \frac{C}{T^2} exp\left(\frac{\phi_b}{kT}\right) \tag{3.3}$$

$$ln\left(R_s T^2\right) \approx ln\left(\frac{C}{T^2}\right) + \frac{\phi_b}{kT} \tag{5.1}$$

In general, analysis of most data sets with both equations gave similar results. Occasionally the full equation was needed in order to produce a good fit to the data. The results of the back contact analysis are shown in table 5.3. The value of ϕ_b is first seen to be ~0.43 eV in the 5 minute sample, where it remained until the 25 minute sample. After this point the barrier height appeared to reduce, but the trend was not consistent across the next four samples. Similar values in a range 0.39 - 0.56 eV have been seen with CdTe cells and Au back contacts which appear dependent on the etching used before application of the metal [6–8]. Macroscopic examination of the 50 minute sample shows significant delamination to the material, with areas of TCO-treated substrate exposed following loss of the sputtered CdS/CdTe layers. Over-treatment with $MgCl_2$ appears to have a detrimental effect on the physical stability of the cell structure, and it is possible that the changes seen in the barrier height with progressive chloride treatment are related to this structural change.

Sample	**Chloride anneal time**	$\boldsymbol{R_s}$ **calculation**	$\boldsymbol{\phi_b}$ eV	**Fit equation**
521/1	0	NA	NA	NA
521/2	5	Slope	0.429 ± 0.003	3.3
521/3	10	Slope	0.425 ± 0.001	3.3
521/4	20	Slope	0.422 ± 0.006	3.3
521/5	25	Single diode	0.34 ± 0.08	5.1
521/6	30	Single diode	0.391 ± 0.005	3.3
521/7	40	Slope	0.32 ± 0.02	3.3
521/8	50	Slope	0.35 ± 0.01	3.3

Table 5.3: The calculated values for the back contact barrier height, ϕ_b for Series 521, with the equation used to calculate R_S and ϕ_b (where 'slope' refers to the method in Appendix B and 'single diode' refers to equation 3.4). In each case the equation chosen produced the best fit as measured through χ^2 and adjusted R^2.

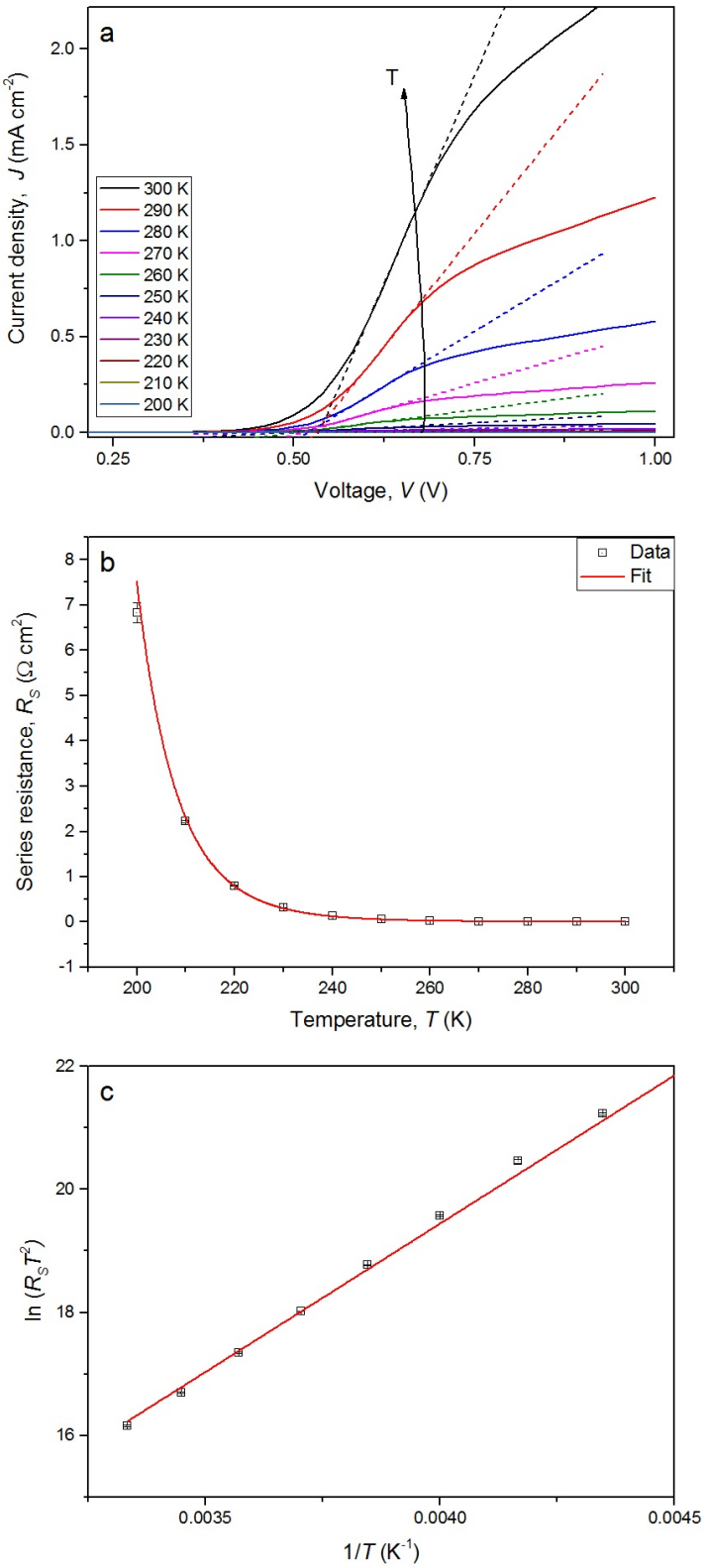

Figure 5.7: Plots to show analysis of the back contact barrier height ϕ_b for Series 521/6 (30 mins); a) Using the slope method (see Appendix B) on a JV curve to find R_S with the linear fits represented by broken lines, and fitting of R_S to b) equation 3.3 and c) equation 5.1.

5.3.1.3 Shallow and deep levels

a) Shallow levels

$C-V$ analysis was used to determine the shallow levels and the depth doping profile as described in section 3.3.2. The operating parameters used are detailed in section 4.3.3. Mott-Schottky graphs of C^{-2} vs V were used to extract information about doping profiles, alongside values for uncompensated acceptor density, N_{nA} and built-in voltage, V_{bi}, through use of a linear fit for the brief linear section at low forward bias voltage (this voltage range is justified in Appendix C). The capacitance at an applied bias of $-1\,\mathrm{V}$ was used to calculate the depletion width, W_D, using the equation $W_D = \varepsilon\varepsilon_0 A/C$, where A is the cell area. The calculated results for these parameters are shown in figure 5.8.

The value of N_{nA} changes with annealing time (5.8 a). The data is noisy and the line is intended as a guide to the eye only. Generally the acceptor density increases from $< 1 \times 10^{14}\,\mathrm{cm}^{-3}$ to $> 2 \times 10^{14}\,\mathrm{cm}^{-3}$ as the treatment time is increased from 0 to 25 minutes, before reducing to $\sim 1.2 \times 10^{14}\,\mathrm{cm}^{-3}$ in the 50 minute sample. These values are in the normal ranges seen for chloride treated CdTe cells (to compare with values of 10^{12} - $10^{15}\,\mathrm{cm}^{-3}$ [9], $\sim 10^{14}\,\mathrm{cm}^{-3}$ [10], 10^{13} - $10^{14}\,\mathrm{cm}^{-3}$ [11]).

Figure 5.8 b) shows the values for V_{bi}, which had a rather high value of 1.6 V for the as-grown sample. It then reduced to $\sim 0.75\,\mathrm{V}$ by 10 minutes before increasing to $> 0.9\,\mathrm{V}$ in the 25 minute sample, after which it fell again to $< 0.85\,\mathrm{V}$. An effect of chloride processing time on the depletion width can be observed in figure 5.8 c), where the 5 minute value (an impossibly large 4.5 µm - thicker than the sample) dropped drastically to a value of 1.65 µm before steadily rising to 2.4 µm by 50 minutes. In the midst of this there appeared to be a sudden drop to 1.4 µm at 25 minutes.

Before interpreting these results, it is worth examining in a little detail the Mott-Schottky plots from which these values derive. These can be seen in figure 5.9. All of the plots in this figure, bar the 0 minute sample, demonstrate a key feature of CdTe solar cells, namely their failure to accurately be modelled by the following equation [12];

$$C(V)^{-2} = \frac{q\varepsilon N(W)}{2(V + V_D)} \tag{3.5}$$

In cells with an abruptly doped junction the plot should be linear, with a negative gradient. The only sample in Series 521 which conforms to this is the as-grown sample seen in figure 5.9 a). However, the frequency at which this result was analysed was 1 kHz, as higher frequency analysis was prone to inductive effects [13]. The inherent danger in analysing the lower frequency range is that

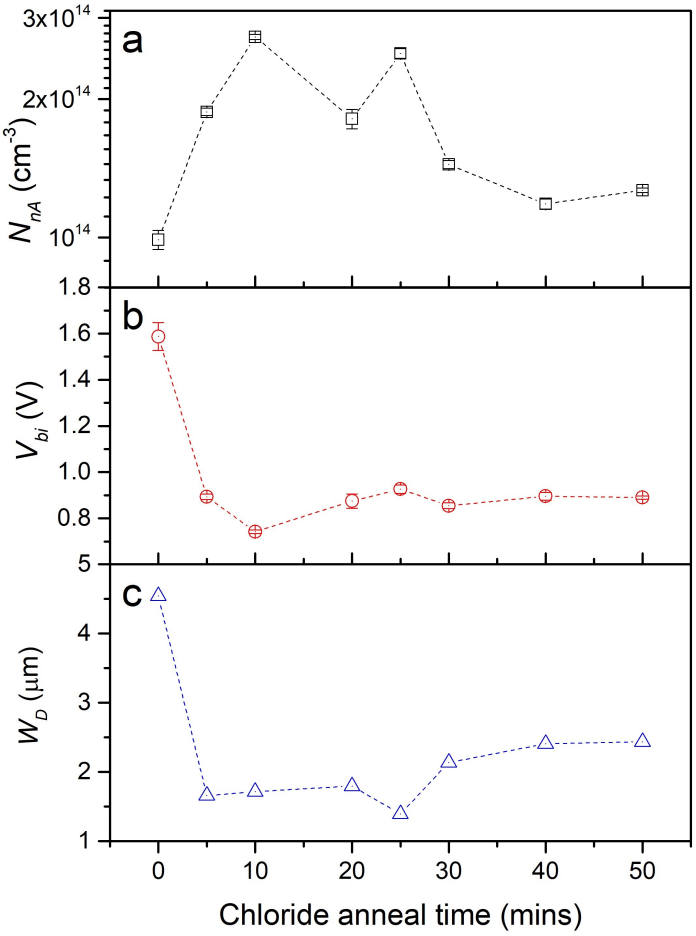

Figure 5.8: Graphs to show values extracted from $C-V$ analysis for Series 521; a) uncompensated acceptor density, N_{nA} ($= N_A - N_D$), b) built-in voltage, V_{bi}, c) depletion width, W_D, calculated from $W_D = \varepsilon\varepsilon_0 A/C$ at -1V. Both a) and b) were calculated from Mott-Schottky plots (see figure 5.9 and Appendix C). The broken lines are a guide for the eye.

traps are likely to be contributing to the capacitance, as discussed in section 4.3.3. This may well contribute to the unphysical extracted value for W_D and by extension N_{nA} and V_{bi} for this sample, and these should be considered to have a large associated error. The results are reported here for completeness. The other cells in this series were able to be analysed at high enough frequencies (100 kHz) for the traps to be unable to respond, and therefore produce reliable results over the linear voltage ranges. Even so, none of the Mott-Schottky plots are linear and are prone to some difficulties in interpretation.

For all the non-optimised samples in this series (5 - 50 minute samples excluding 25 minutes) there was still a dependence of capacitance on voltage evident at -1 V bias, indicating that the cells were not fully depleted at this voltage. The gradients of their slopes also varied, implying a spatially varying N_{nA}. (The 25 minute sample was again anomalous and behaved as if there was a fully de-

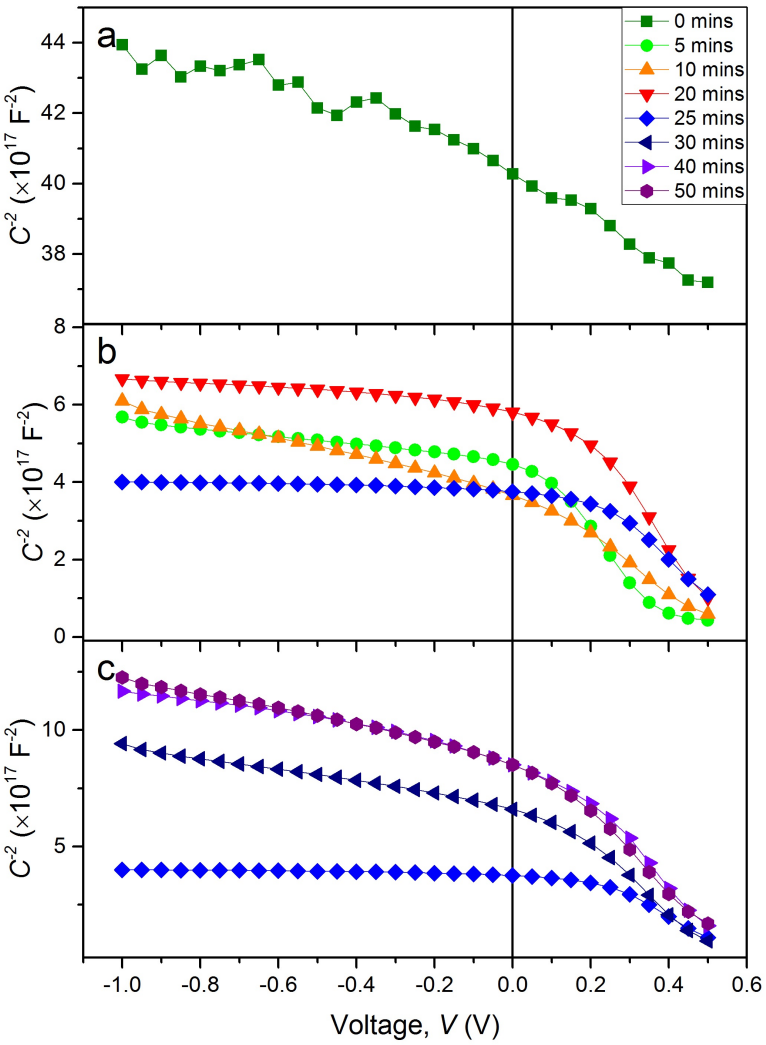

Figure 5.9: A comparison of the Mott-Schottky plots for Series 521 samples, a) 0 mins, b) 5 - 25 mins, and c) 25 - 50 mins. The graph for 25 mins is similar in appearance to the typical a-Si $p - i - n$ diode [12].

pleted space charge region as is typical of $p-i-n$ amorphous silicon (a-Si) devices [12].) The voltage range over which a linear fit was used to calculate the above parameters greatly affects the results. This is discussed in more detail for this series in Appendix C. Indeed, without corroborative analysis methods such as drive level capacitance profiling (DLCP) or illuminated CV analysis, it is difficult to ascertain with full confidence the correct values for all the devices studied here, although dark $C-V$ analysis is often used for CdS/CdTe cells in this manner [9, 13–16].

Another way to compare the samples is from the local slope at all voltages so as to produce a depth-density profile of doping. A comparison for Series 521 is seen in figure 5.10. The first panel shows how the bias voltage probes different areas of the space charge region, with the reverse bias probing the bulk of the depletion width and being responsible for the left-hand side of the 'U'. The low- to mid-forward bias produces values for the right-hand side of the curve. High forward biases ($\gtrsim 0.5\,\mathrm{V}$) are excluded from the analysis as they produce an increased capacitance component from the back contact that is not related to carrier density [17].

The samples which have been optimized and over-treated shown in figure 5.10 c) demonstrated the 'U' shape commonly seen in CdTe cells. The evolution of this 'U' from the comparatively flat as-grown sample is shown in 5.10 b), with the left-hand side of the 'U' developing an increase in N_{nA} near the CdS/CdTe interface. The right-hand branch of the curve is often interpreted as a result of non-uniform carrier density and is sensitive to the effects of deep trap levels; with increasing negative bias, the resulting band-bending expands the separation of E_F and E_V, and forces some deep levels beneath E_F. When occupied by electrons they then contribute to the space charge in an identical way to the shallow levels. The observed carrier density from such plots may therefore include the trap density alongside the shallow levels. A consequence of this would be for N_{nA} to increase with negative bias [14]. This is evident in the plot for the 25 minute sample in figure 5.10, and will be referred to in the following section on deep levels. The effects of deep traps could also contribute to the bottom of the 'U' shape, giving an overestimation of shallow doping.

From the depth density profile in figure 5.10 it appeared that there is an overall comparative increase in the doping for the 25 minute sample across the full space charge region (disregarding the noisy and oddly shaped curves for the weakly treated samples). It may be speculated that the $p-i-n$ appearance of this sample's Mott-Schottky curve may indicate less homogeneous doping across the cell, which would accord with the high levels of doping seen in figure 5.10 c) at $W_D(\mathrm{norm}) \approx 1$, although there are alternative explanations which will be

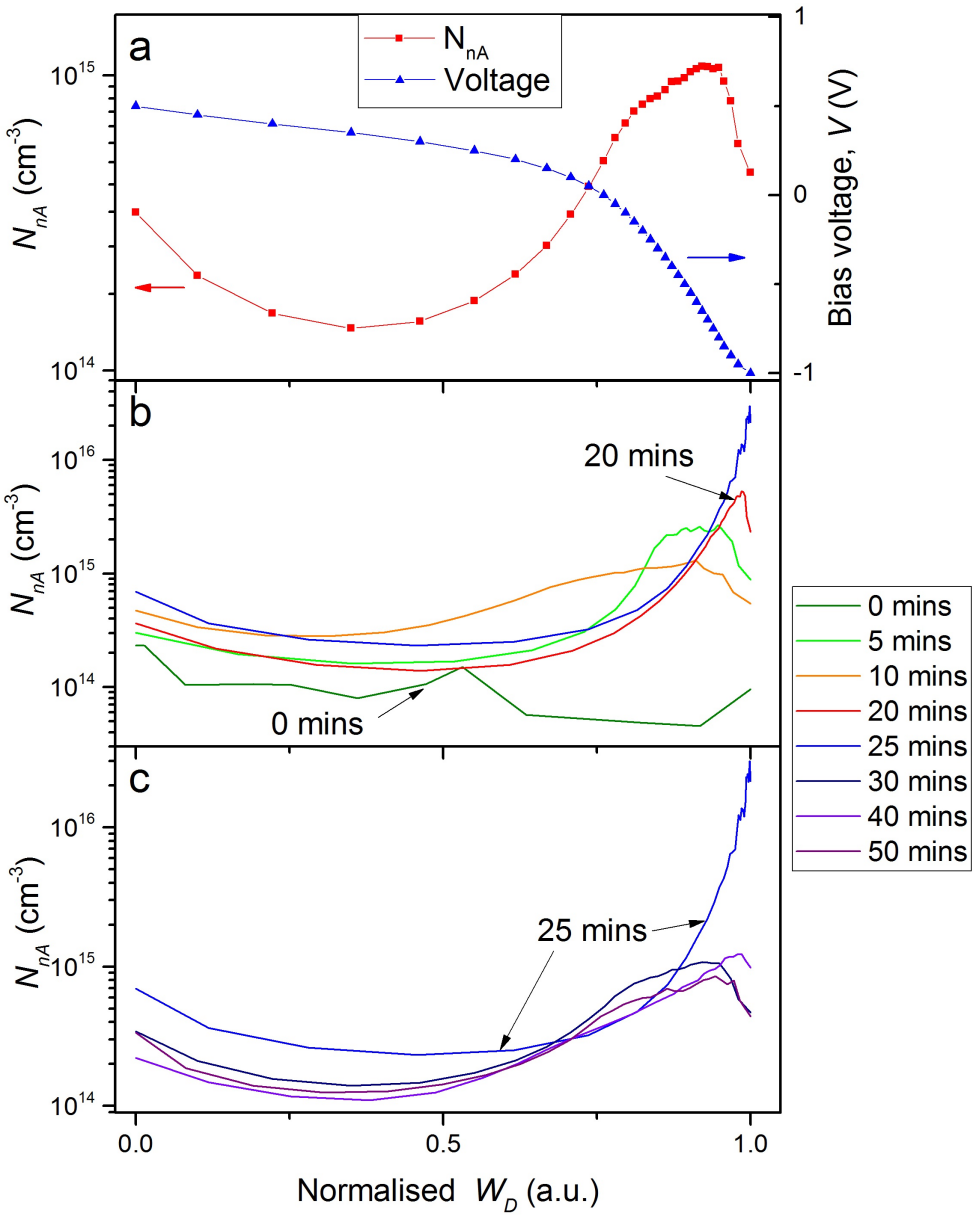

Figure 5.10: Plots to show the normalised depletion width, W_D vs the uncompensated acceptor density, N_{nA} (doping density plots) for Series 521. Figure a) demonstrated how the bias voltage corresponded to the depth profile for the 30 minute sample as a typical example. Figures b) shows data for sample processed from 0 - 25 minutes, and c) for 25 - 50 minutes.

discussed shortly. The fully depleted nature of this plot even at 0 V bias could indicate a phenomenon called 'reach-though', where the capacitance was now being determined by the highly-doped CdS layer. However if that were indeed the case, it would be expected that the calculated value for N_{nA} would be greater ($> 10^{17}\,\mathrm{cm}^{-3}$) than those observed.

b) Deep levels

The behaviour of deep levels as a function of chloride treatment time was studied using Thermal Admittance Spectroscopy (TAS). The methodology and practical parameters were described in section 4.3.4.2 following the theory in section 3.3.3. A worked example can be found in Appendix A. The analysis provided energy values for apparent trap levels, E_{nA}, alongside trap densities, N_{nt} and capture cross-sections σ_{nA} [section 3.3.3] as shown in figure 5.11. Series 521 was studied at five voltage biases in order to obtain further information about trap spatial distribution as shown in figure 5.12.

Firstly a description of the zero bias results. In figure 5.11 a) the apparent trap energies E_{nA} are shown. It is clear that the energies varied as a function of chloride processing time. In the as-grown sample there were two traps at (0.210 $\pm$ 0.013) eV and (0.005 $\pm$ 0.002) eV. Despite these traps having very small cross sections ($< 10^{-21}\,\mathrm{cm}^{-2}$) the values otherwise corresponded reasonably well with traps observed in untreated[1] CdTe. Three traps in the same energy range are $\mathrm{Cu_{Cd}}$ (-1) {0.22 eV} [2], $\mathrm{V_{Cd}}$ (-2) {0.21 eV} , $\mathrm{Na_{Cd}}$ (-2) {0.02 eV} [20]. Other traps reported for single crystal p-CdTe in this range include also a low energy (0.06 $\pm$ 0.05) eV [21] trap, 0.20 eV, and 0.10 eV [22].

The lower energy level observed will be discussed first. There have been a number of reports of similar low energy levels in single and polycrystalline CdTe devices, thought to be caused by contaminants such as Na from the substrate glass. A low energy peak was present for the 0 and 5 minute treated samples (see figure 5.11). This peak was also measured across the voltage bias range from $-0.3\,\mathrm{V}$ to $0.9\,\mathrm{V}$, indicating that the defect was homogeneously distributed across the depletion region. The average energy of the measured low energy peak across all voltage biases was (0.005 $\pm$ 0.004) eV in the 0 minute sample, and (0.018 $\pm$ 0.003) eV in the 5 minute sample. However, this peak disappeared for longer treatment times. Perhaps this was a chemical effect of the chloride treatment process, although it is possible that other traps came to dominate the admittance spectrum rendering the low energy peaks no longer visible with TAS.

The second of these two levels seen in the 0 minute device has a starting value of (0.210 $\pm$ 0.013) eV at 0 V bias (figure 5.11). This was also visible in reverse bias as seen in figure 5.12 with a level of (0.199 $\pm$ 0.016) eV. However in forward bias it is no longer visible, and the admittance spectrum was instead dominated by a large peak with an energy of ~ 0.49 eV at 0.3 V bias, increasing to

[1] The purity of thin film and single crystal CdTe is often low, with common impurities including Cu, Na, As, Ag, P and Li [18, 19].

[2] This nomenclature indicates a Cu atom on a Cd lattice site with an ionisation charge state of -1, and an activation energy (E_A) of 0.22 eV.

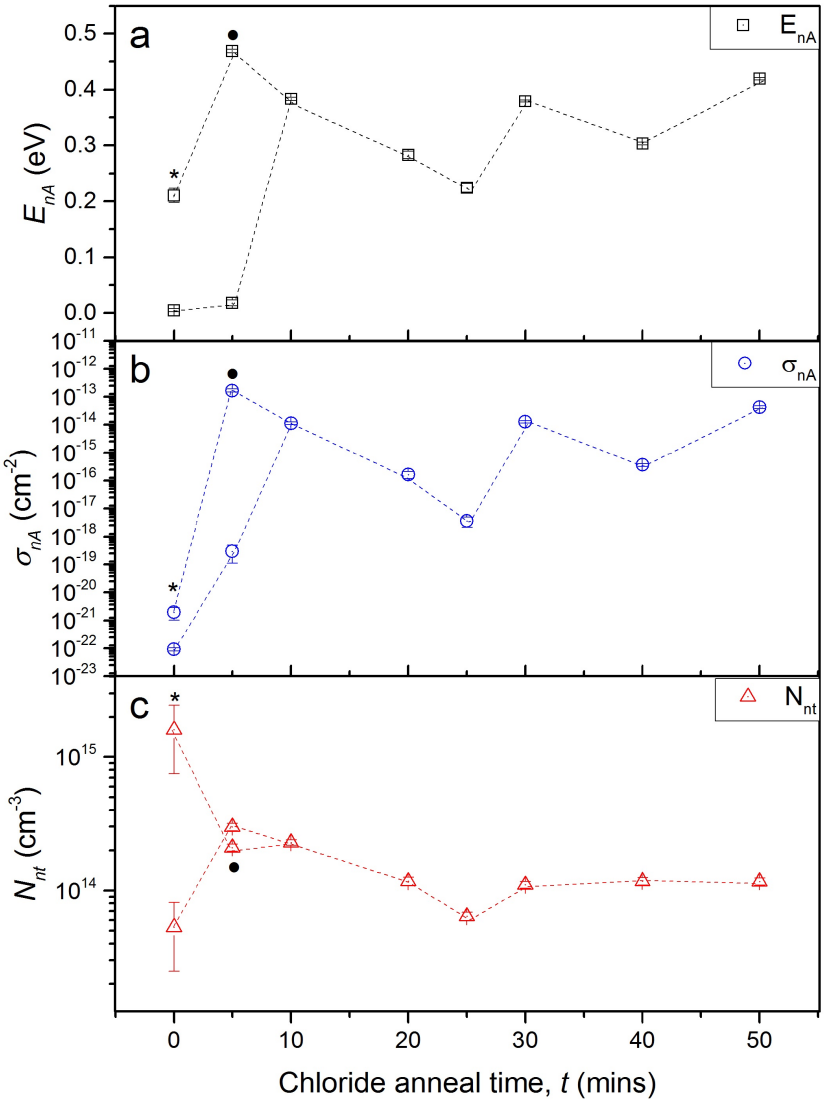

Figure 5.11: Apparent trap parameters of Series 521 at 0 V bias, as determined through TAS; a) apparent trap energy, E_{nA}, b) apparent cross section, σ_{nA} and c) apparent trap density, N_{nt}. The broken lines are a guide for the eye, and where two traps are present for a given treatment time one of the is marked with an asterisk or dot to allow identification between plots.

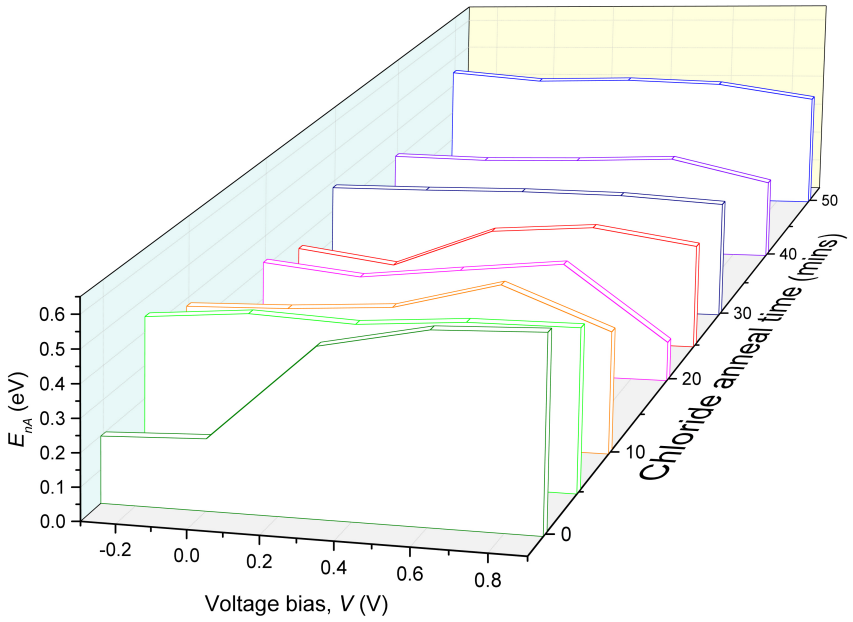

Figure 5.12: Plot showing the change in apparent trap energy, E_{nA}, as a function of voltage bias applied during data collection. (The shallow trap seen in figure 5.11 is omitted.) Five different voltage biases were applied, from $-0.3\,\mathrm{V}$ to $0.9\,\mathrm{V}$ in steps of $0.3\,\mathrm{V}$. The most profound changes are for the unprocessed sample (0 minutes).

$\sim 0.56\,\mathrm{eV}$ at $0.9\,\mathrm{V}$. It is possible that the deeper $\sim 0.5\,\mathrm{eV}$ trap obscured the $0.21\,\mathrm{eV}$ trap signature, as the small admittance signal in this sample made analysis of fine features difficult. The increasing value of the deeper trap at higher forward voltages implies an interface state [23]. In optimised (chloride treated) devices the electrical junction is moved towards the front of the cell (i.e. towards the CdS junction) but is still just within the CdTe [24]. Unlike the optimised device, the electrical junction in this as-grown material is entirely within the bulk of the CdTe, and there are two possible interfaces; the CdS/CdTe junction and the CdTe/Au back contact. However, although parasitic back contact effects were evident in the $J-V$ curves of all the chloride treated cells (i.e. rollover), this was not the case with the as-grown sample, even at $1\,\mathrm{V}$ of forward bias. This implies the trap visible at $0.9\,\mathrm{V}$ was not within the back contact region, which is likely to be the case for almost all the chloride treated samples.

The 5 minute sample showed a consistently deep trap $\sim 0.46\,\mathrm{eV}$ which is invariant across the voltage bias range. This is likely to be the same trap as visible in the forward voltages of the as-grown sample, as it demonstrates similar energy, cross section ($10^{-14}\,\mathrm{cm}^{-2}$) and trap density ($1 \times 10^{14}\,\mathrm{cm}^{-3}$). However the energy level was more stable across the bias range, and with an average value of (0.462 ± 0.012) eV it was slightly shallower than in the as-grown sample. At zero bias, the

10, 20 and 25 minute samples showed a progressive decrease in E_{nA} with treatment time (which was mirrored in both σ_{nA} and N_{nt}) to a minimum of (0.224 ± 0.008) eV at 25 minutes. For these three samples, the bias dependency showed an increase in trap energy to a maximum value at 0.6 V, which may indicate either an energy or spatial distribution of trap energies being sampled.

For the three over-processed samples (30, 40 and 50 minutes) E_{nA} started to increase again with processing time, with corresponding increases in σ_{nA} and N_{nt} as seen in figure 5.11. The extracted parameters did not vary significantly as a function of bias, implying a homogeneous distribution across the space charge region. The increasing energy values corresponded with a reduction in cell performance as seen in figure 5.1.

The trap behaviour of the under-processed cells is now discussed. The 10 minute sample demonstrated a comparatively steep increase in observed trap energies with increasing bias voltage. This sample also displayed significant shallow doping inhomogeneity across the depletion width in the doping profile (see figure 5.10), with lower levels of N_{nA} evident at forward bias rather than reverse. It is speculated that these two parameters are directly connected, and the variation of trap energy with bias does not imply an interface state in this sample, but rather an inhomogeneity in the chemical composition of the local lattice. This feature was less pronounced in the 20 minute sample, except for another drop in E_{nA} at 0.9 V.

In the 25 minute sample shallower traps were observed at reverse and neutral voltages, but deeper levels in forward bias. The low E_{nA} for the 20 and 25 minute samples in reverse bias could also in part account for the sharp rise in apparent doping on the right-hand side of the 'U' in figure 5.10: as discussed in in the previous section, levels below E_F will contribute to the space charge in a way similar to shallow levels. If the benefit of chloride treatment is a general reduction in trap energies (as appears to be the case here) there are likely to be more traps contributing to the capacitance in reverse bias for these samples, which may explain the shape of their doping profiles.

5.3.1.4 Equivalent circuit

In this section the samples in Series 521 were investigated using AC equivalent circuit methodology as described in section 4.3.4.3.

In the analysis that follows, a variety of alternative equivalent circuits were tested as seen in figure 4.3. The circuits used were described in table 4.2 on page 70. In brief, the models (a - i) start from a basic single diode model (a) and increase in complexity, with more components in each subsequent model. The

panels on the left hand side of figure 4.3 (namely a, d, g and h) show examples of models where the main $p-n$ junction dominates the capacitance and admittance behaviour of the cells. On the right hand side of the same figure are examples which include other compounding electrical effects such as a Schottky barrier at the back contact (b, c and e) [25] or grain boundary contributions (e, g and i) [1]. Models (h) and (i) are similar to models (f) and (g) respectively, each containing additional parallel $C_i - R_i$ (i=1 - 3) pairs representing different trap responses. In general it is easier to produce a good fit to experimental data with more components in the circuit. As such, circuit models which produce a good fit with the fewest components are thought more likely to represent the true cell operation. [Models 'h' and 'i' from figure 4.3) are not included in the following discussion as fits were not possible without producing unphysical component values.]

For Series 521 the equivalent circuits were modelled using capacitance data taken at three DC bias voltages, 0 V, 0.3 V, and 0.6 V. These voltages were chosen as a) they cover the working range of the device, and b) trap parameters had been calculated for these biases. In order to visualize the accuracy of the fit, the complex parameters of dielectric permittivity, ε^*, and electric modulus, M^*, were used as these have been found to be more sensitive to fit parameters [7]. These values are related to the impedance Z^* as below;

$$M^* = j\omega C_0 Z^* \tag{5.2}$$

$$\varepsilon^* = \frac{1}{M^*} \tag{5.3}$$

where

$$C_0 = \varepsilon_0 A/t \tag{5.4}$$

In these equations A is the area and t is the film thickness. For the data collected, the capacitance of the equipment, C_0, is not precisely known, so the relative electric permittivity, $\varepsilon^* C_0$, and the relative modulus, M^*/C_0 are used. Fit quality is determined by the sum of the squares of the residual, R^2. An example of different fit qualities is shown in 5.13 in which model 'c' gives the best fit.

A summary of the fit quality for the models applied to all samples in Series 521 is shown in table 5.4 for DC biases of 0, 0.3 and 0.6 V. It can be seen that there are several circuits which provide a good fit to the data. Four models produce better fits than others, namely 'c', 'd', 'f' and 'g'. It is evident that there are differences between the quality of fits obtained and the voltage bias at which admittance data was taken. Models 'f' and 'g' were discarded as candidates for

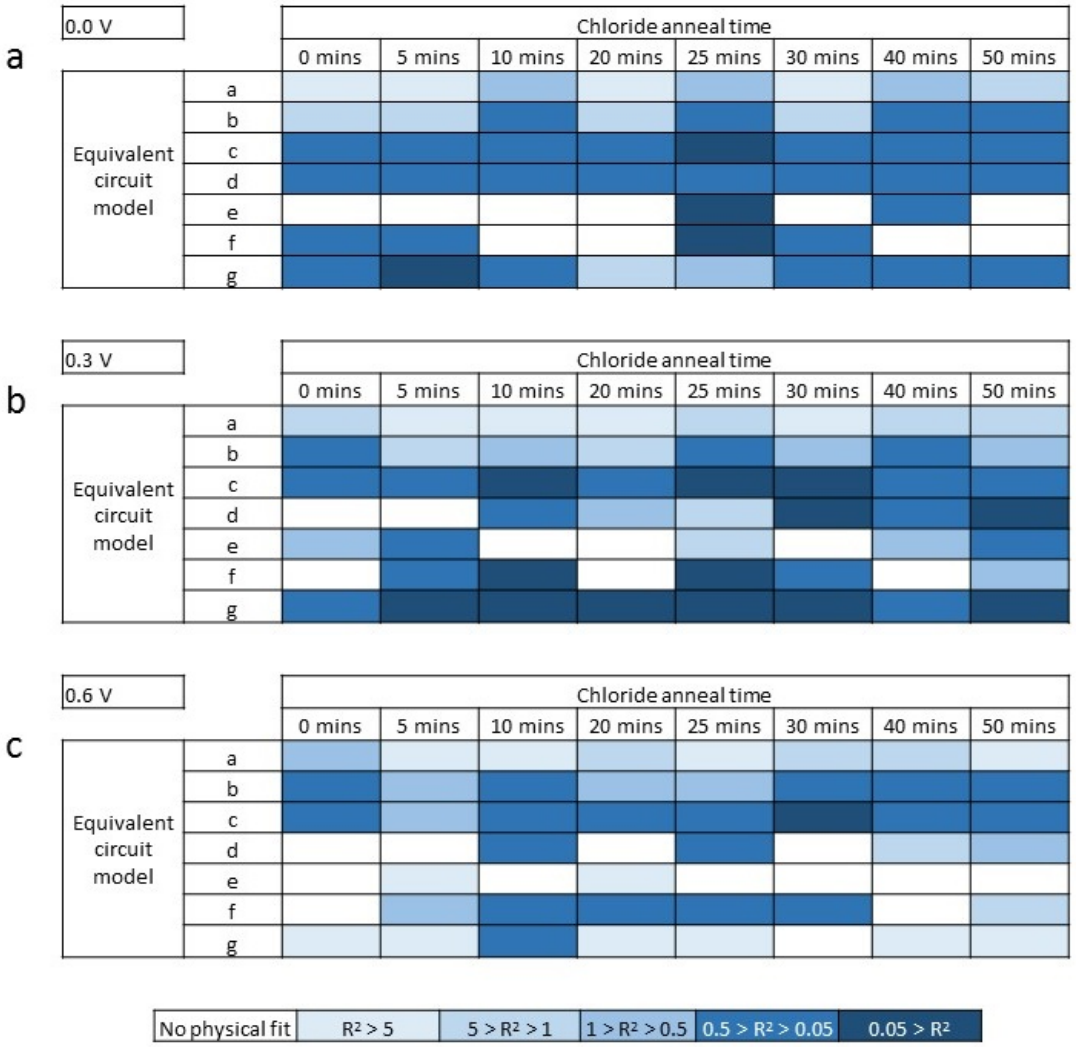

Table 5.4: A schematic to show the range of fit quality for equivalent circuit models a - g (see figure 4.3) to admittance data at a) 0 V, b) 0.3 V and c) 0.6 V for Series 521. The fit quality is indicated by a colour gradient corresponding to R^2, which is the sum of the squares between the data and the fit value. Fits which do not converge, or provide unphysical circuit components are shown in white.

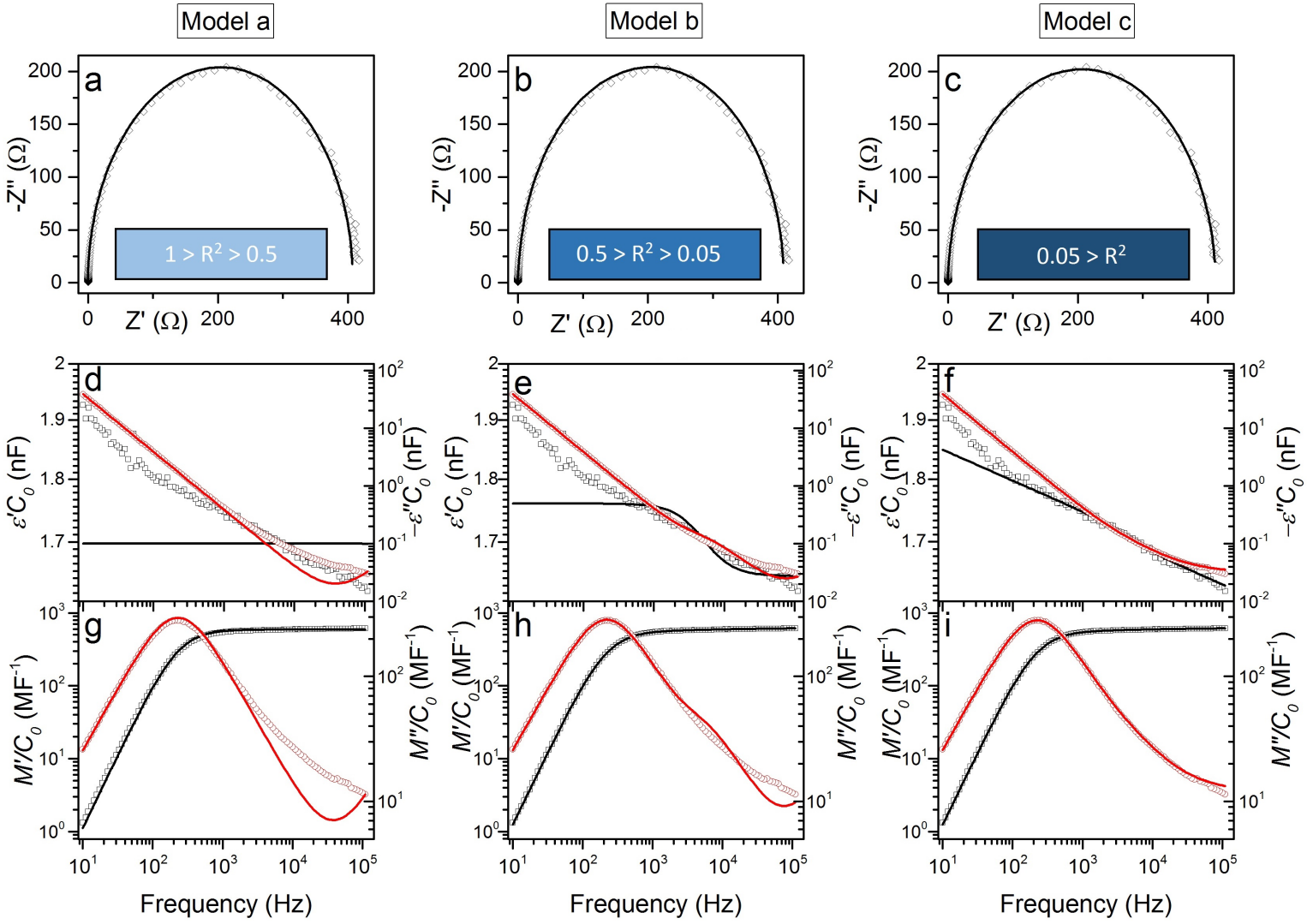

Figure 5.13: A typical example of fits of circuit models to experimental data, in this case for sample 521/5 to the circuits 'a' (panels a, d, and g), 'b' (panels b, e, and h), and 'c' (panels c, f, and i) from figure 4.3. The data is denoted by symbols and the fits represented by lines. The parameters shown are a Cole-Cole plot in panel a, b, and c, relative dielectric permittivity vs frequency in d, e, and f, and relative electric modulus vs frequency in g, h, and i.

all samples, as there were simpler circuits which provided excellent fits. Model 'c' produced good quality fits across most samples at both voltages, but tended to fail to describe the low frequency behaviours accurately. For the 0 bias voltages model 'd' produced a more accurate representation across the frequency range. However, as it appears unlikely that the equivalent circuit design would change as a function of DC bias, the model 'c' was thought to be most representative for all of Series 521.

The graph in figure 5.14 a) compares the values for R_S as calculated using

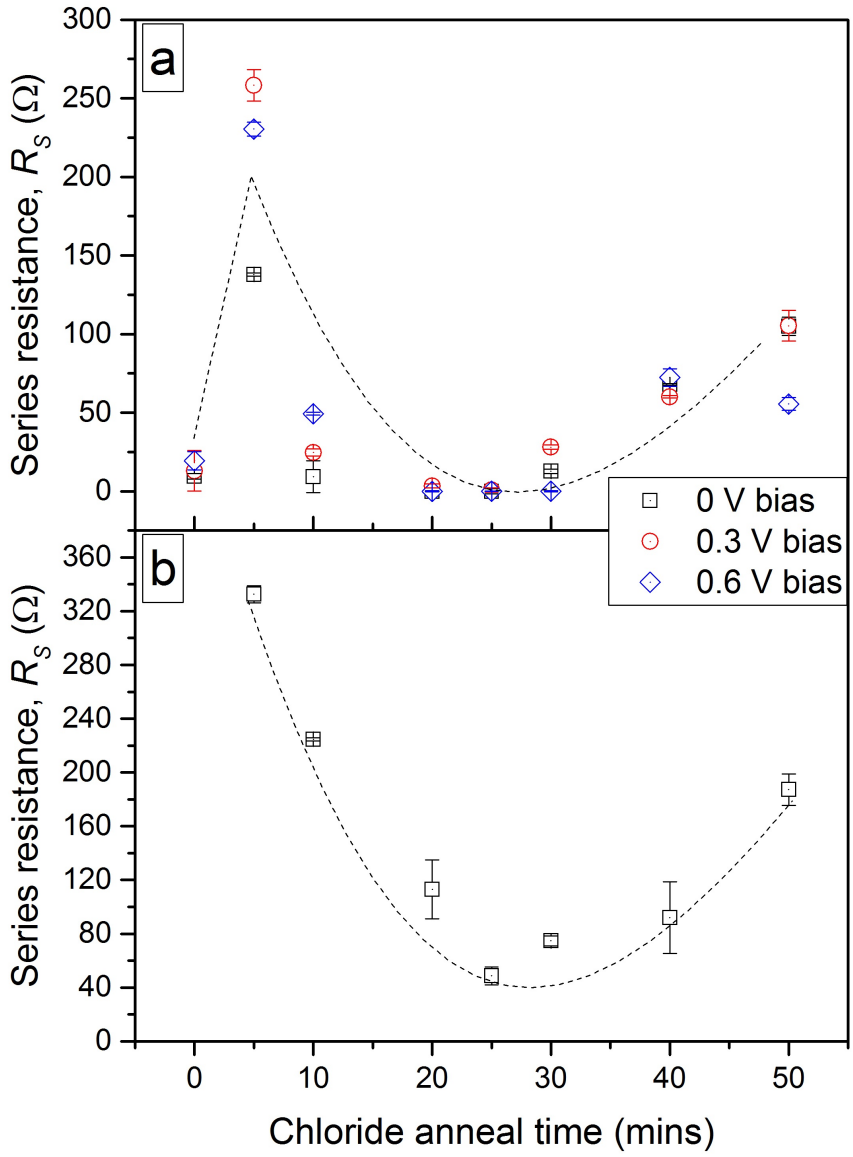

Figure 5.14: The variation of R_S with chloride anneal time, a) the results from fitting the admittance data for Series 521 using circuit model 'c' from figure 4.3, at different bias voltages, b) the values calculated by the slope method using $J-V-T$ data at 300 K as comparison. Although the calculated values are greater in b) than a) the trend is similar.

model 'c'. From analysis at all three DC biases a similar 'U' shaped trend can be seen. The as-grown device demonstrated a low value of R_S ($\sim 15\,\Omega$) which increased drastically within 5 minutes of treatment to $\sim 200\,\Omega$. This early peak was followed by a 'U' shaped curve with a minimum at the 25 minute sample. This trend was comparable to that seen using calculated values of DC R_S from $J-V-T$ data, which can be seen in figure 5.14 b).

Is is concluded that initial application of chloride treatment acted to change the R_S drastically, after which there was a reduction through the process of chloride annealing. Prolonged treatment beyond optimisation increased the resistance again. The saddle point in these plots has insufficient data points to indicate if the change from decreasing to increasing R_S was abrupt or gradual. The former may be an indication of two separate processes happening in conjunction, one of which was beneficial to the cell, and the other detrimental. Alternatively it could be related to a saturation process where over-saturation introduces new defects.

5.3.1.5 Summary of results for Series 521

The following statements summarise the results from analysis of Series 521.

- The performance of CdS/CdTe devices processed with $MgCl_2$ was dependent on the length of treatment time, with there being a sharp onset of improvement followed by a broad peak in performance followed by a slow decline with over-treatment. The best performing cells combined high V_{OC}, J_{SC}, and FF.

- The peak in solar cell performance corresponded to a sharp local maximum in acceptor density. This also corresponded to minima in the deep level energy, density and cross sections.

- Current transport analysis indicated that the multi-step tunnelling mechanism could be fitted to the temperature dependent $J-V$ data for $T > 250\,\mathrm{K}$. Moreover the number of tunnelling steps was at a minimum for the best performing cells. However, the best performing device (25 minutes) had different behaviours - the multi-step model did not fit well, the $C-V$ response was reminiscent of $p-i-n$ behaviour, and R_S was exceptionally low.

- The AC response of all devices was best fitted to equivalent circuit model 'c' (4.3) comprising an $R-C$ segment (possibly the main junction), $R-CPE$ component (possibly a distribution of traps and grain boundaries) and a series resistance.

- The contact barrier height was invariant with processing (at ~0.45 eV) until the samples were over-processed and the layers broke down.

5.3.2 CdTe cells with CdS:O window layer having varied $MgCl_2$ treatment times (Series 522)

5.3.2.1 Performance data

a) Efficiency and working parameters

The sample plates from Series 522 were analysed under AM1.5 illumination to extract performance parameters. Figures to show the result for samples air annealed with $MgCl_2$ at 410 °C are shown in figure 5.15, while those annealed at 390 °C are in figure 5.16.

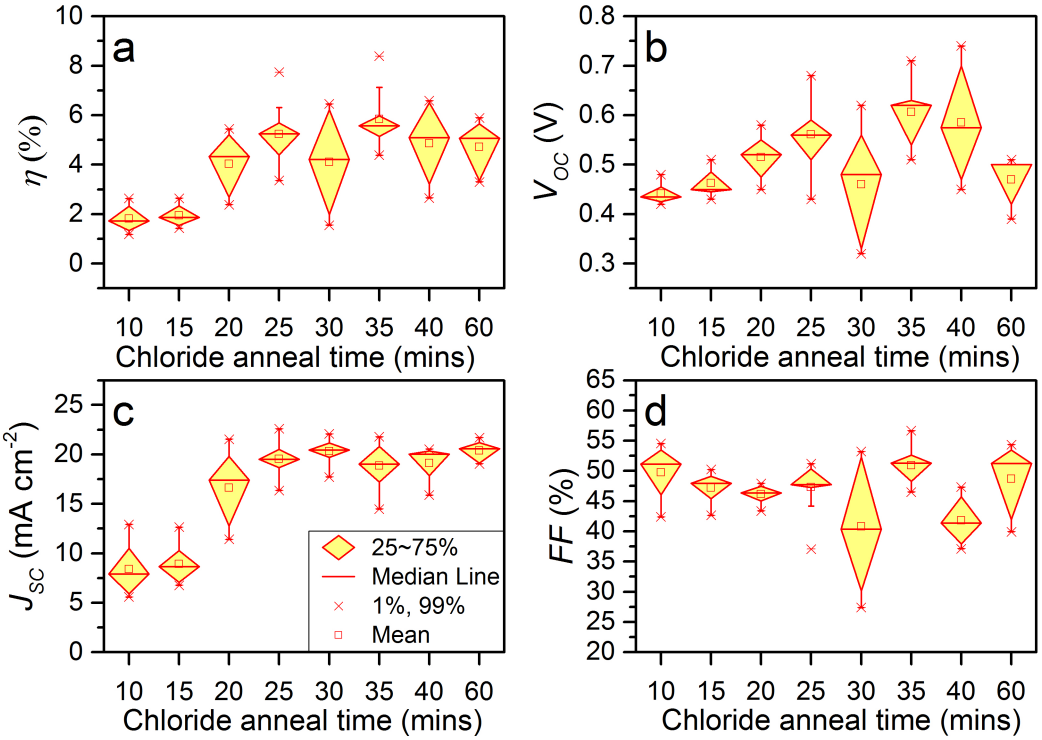

Figure 5.15: Box plots demonstrating the spread of performance parameters for N contact dots (max $N = 9$) on CdS:O/CdTe devices as a function of chloride treatment time (Series 522) processed at 410 °C, showing a) efficiency η, b) open circuit voltage V_{OC}, c) short circuit current density J_{SC}, and d) fill factor FF. There was a local maximum in parameters in the 25 - 35 minute region (the point at 30 minutes is a bad data point - see text).

Inspection of figure 5.15 shows a gradual improvement in η from ≈ 2 after 10 minutes of treatment, to $4-8$ between 25 and 35 minutes. The 30 minute sample

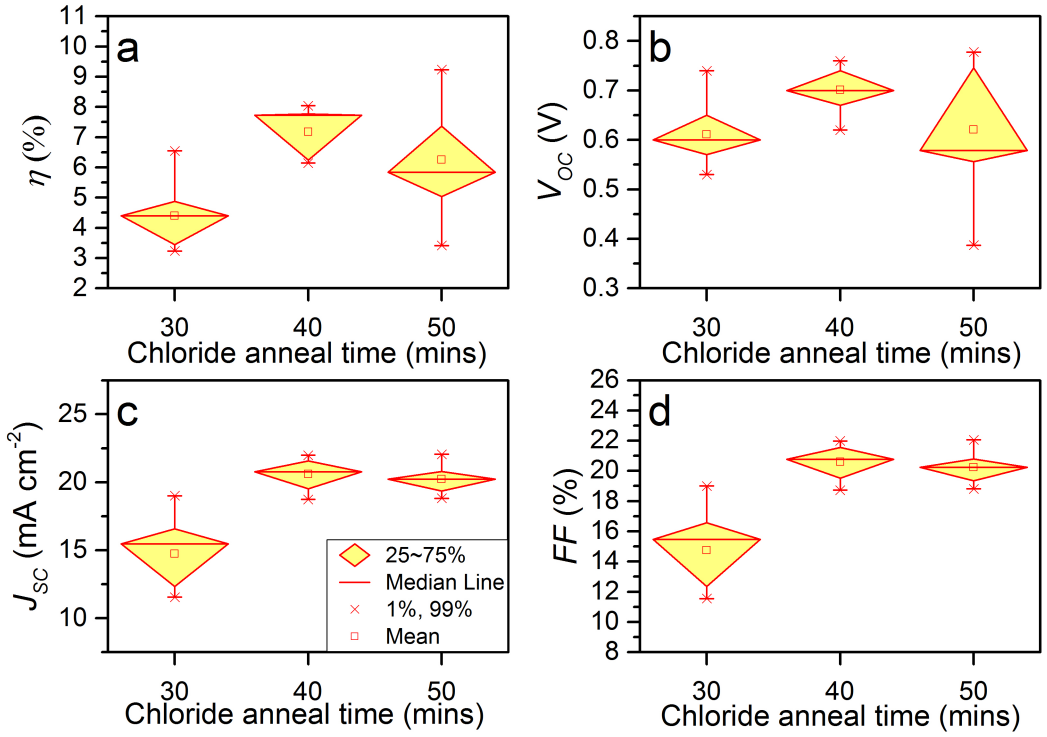

Figure 5.16: Box plots demonstrating the spread of performance parameters for N contact dots (max $N = 9$) on CdS:O/CdTe devices as a function of chloride treatment time (Series 522) processed at at 390 °C, showing a) efficiency η, b) open circuit voltage V_{OC}, c) short circuit current density J_{SC}, and d) fill factor FF. Local maxima are seen in all plots for 40 minutes of $MgCl_2$ annealing.

has lower performance parameters than the overall trend would suggest and is considered to have generated a bad data point. A similar pattern is apparent in V_{OC}, with a gradual improvement to values > 0.6 V at the peak of performance. J_{SC} rose markedly after 20 minutes where it reached a plateau. The FF graph showed no significant variation as a function of treatment time. For these samples the most optimised device was seen at 35 minutes of $MgCl_2$ processing.

For the samples in figure 5.16 (390 °C) a peak in all performance parameters was evident at 40 minutes. With a cooler annealing temperature than the the rest of the series, it would be anticipated that a longer processing time would be required to effect the chloride-induced improvement, if there was a thermally activated aspect to the process (this latter point is explored in detail in section 6).

Examples of the illuminated $J-V$ curves for Series 522 are shown in figure 5.17. In the upper panel a progression can be seen from 10 to 60 minutes. The J_{SC} increased from ~ 10 mA cm^{-2} and quickly reached the maximum of > 20 mA cm^{-2}. The V_{OC} increased from 0.49 V to 0.71 V between 10 and 35 minutes of processing, before decreasing again to ~ 0.71 V by 60 minutes. The improvement appears to

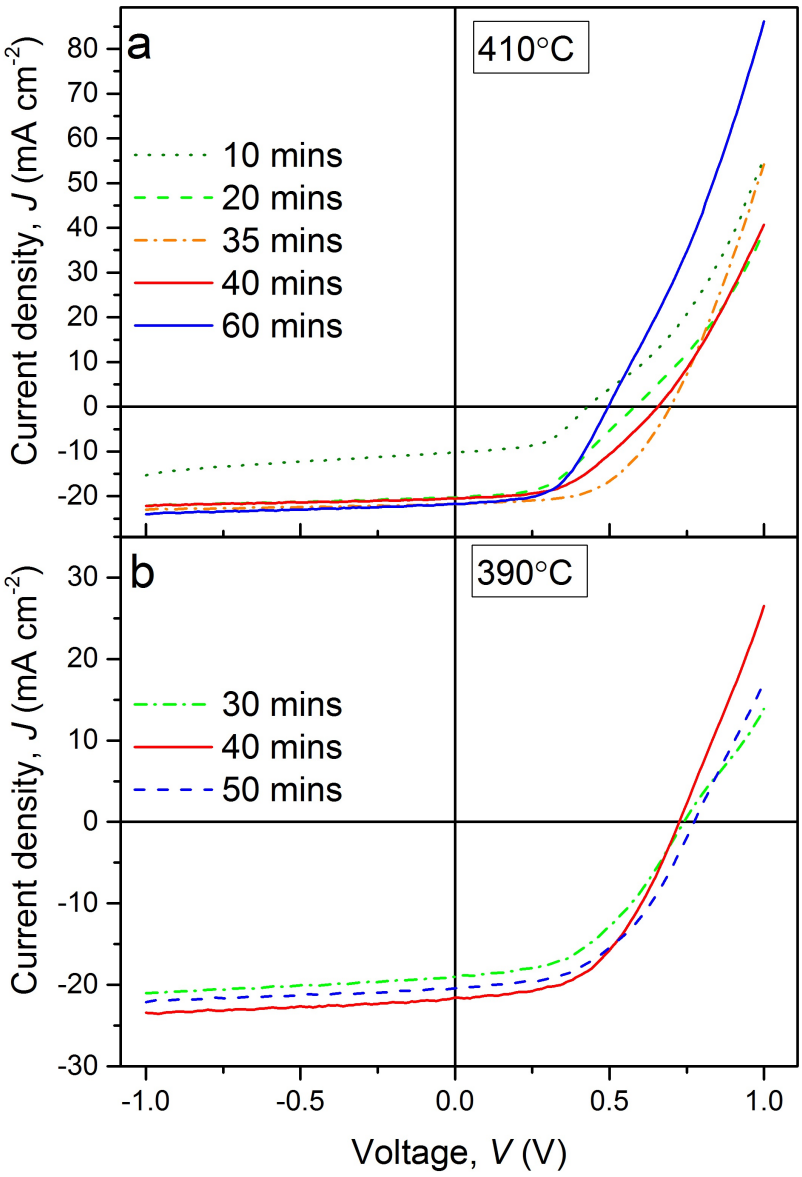

Figure 5.17: Typical $J-V$ curves for CdS:O/CdTe devices processed with $MgCl_2$ for various times at a) 410 °C, and b) 390 °C.

be related to a reduced R_S and a shifting of the maximum power point to higher voltages, although this had almost reversed in the 40 minute sample. For some samples the curves also had a different appearance to those typically seen, insofar that the high forward voltage (> 0.75 V) was associated with a *reduction* in R_S, rather than the usual increase seen in rollover. This effect was particularly visible in the 10 and 60 minute samples. The graph in panel b) shows the slides processed at 390 °C, and this unusual shape does not appear to be replicated here. The 40 minute sample demonstrated the highest J_{SC} at 21.5 mA cm^{-2}, but the lowest V_{OC} of the three plots at 0.72 V. The R_S was lowest in this plot however, and none of these three samples demonstrated any rollover in high forward bias.

b) EQE

Figure 5.18 shows EQE data for Series 522. A progressive improvement can be seen in the samples processed at 410 °C from 10 minutes onwards, reaching optimal performance by 35 minutes, with little change thereafter. From short to long frequencies, the features seen are;

- The is a shift in the lower band edge to ~3.6 eV, which is in the range seen

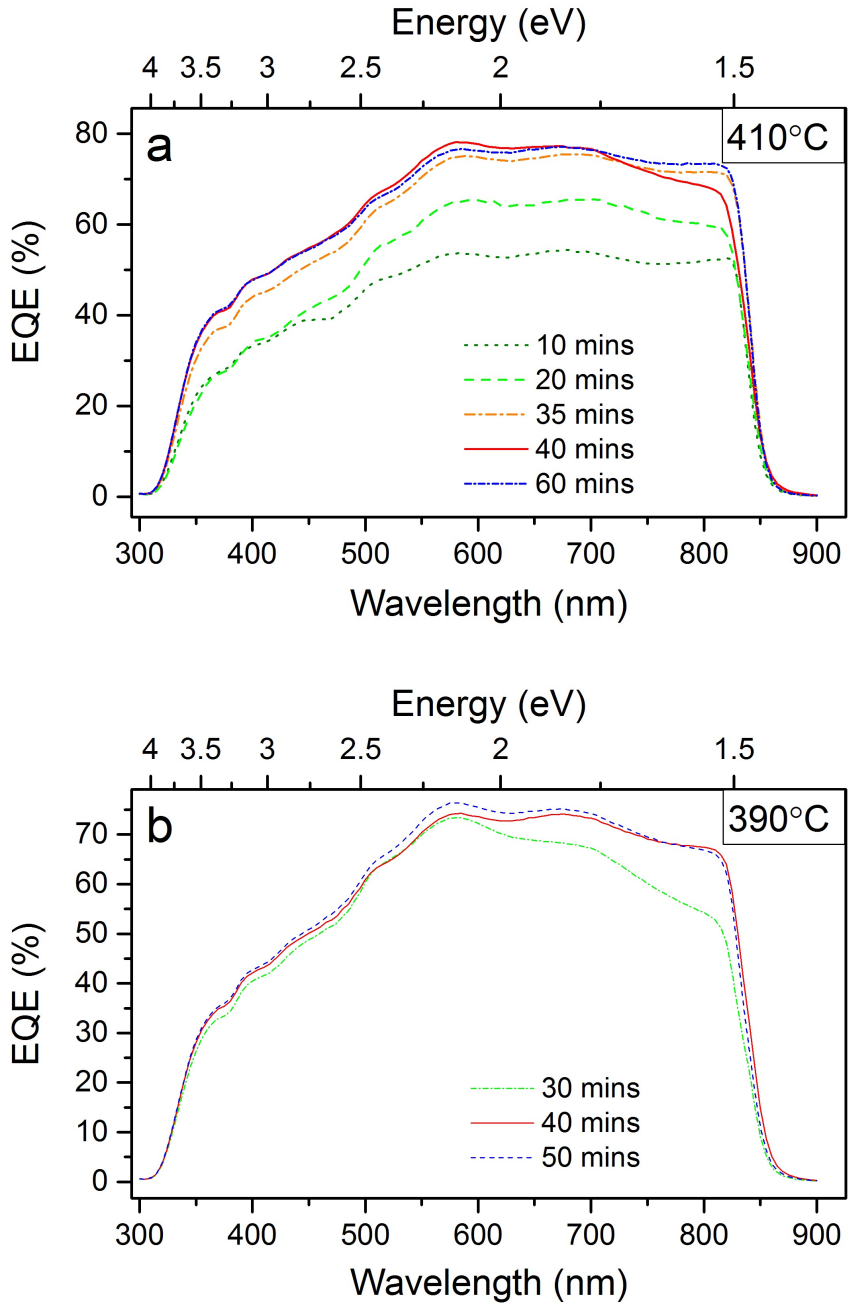

Figure 5.18: Typical external quantum efficiency (EQE) profiles for Series 522, CdS:O/CdTe samples processed with $MgCl_2$ for the stated times and at temperatures of a) 410 °C, and b) 390 °C.

for CdS:O thin films [26],

- Short wavelength (350 - 500 nm) changed from those seen in CdS devices, with increased generated current from these high energy photons, a feature typical for CdS:O devices [27],
- A comparatively invariant EQE from 580 - 830 nm, indicating a heterojunction with improved absorption of the longer wavelength photons, with little change between the samples processed from 35 - 60 minutes (this is in keeping with the slow reduction of J_{SC} seen in figure 5.15 c).

The samples processed at 390 °C had the same features as described above, with the 40 and 50 minute cells showing similarly increased absorption at the longer wavelengths. As seen in the other samples, this was in keeping with their comparable J_{SC} values seen in figure 5.16 c).

5.3.2.2 Current transport

a) Main junction

$J-V-T$ analysis results are shown in figure 5.19 for samples processed at 410 °C and figure 5.20 for those processed at 390 °C. The upper panels of figure 5.19 show the raw $J-V-T$ data. In panels a) and c) the shapes of the 10 and 60 minute samples curves were again unusual, with an additional linear section present in the 0.5 V region (see circles on plots). This effect was more pronounced in the 60 minute sample. The more optimised samples did not have this feature, as seen in panel b). Unfortunately, the best performing sample plate for this series (35 minutes) was damaged by the measuring process, and no useful $J-V-T$ data obtained. The samples processed at 390 °C did not show the unusual $J-V$ curve shape (an example is shown in 5.20 d), but again the 50 minute sample was damaged and no useful $J-V-T$ data procured.

As with Series 521, the samples in 522 were first analysed for evidence of multi-step tunnelling using equation 2.12. The results of this are shown in figure 5.19 d - f (samples processed at 410 °C) and 5.20 b - d (for those processed at 390 °C). In panel 5.19 d) a progression of $ln\, J_0$ with treatment time can be seen, with under- and over-processed samples having J_0 values of $\sim 3 \times 10^{-10}$ mA cm^{-2} ($ln\, J_0$ of -22 to -23) at 300 K which increased to $> 5 \times 10^{-9}$ mA cm^{-2} ($ln\, J_0 >$ -20) in the samples processed between 20 and 30 minutes. All of the samples demonstrated decreasing values of J_0 with temperature, as expected for this temperature activated current. In panel e) [which shows a variation of the parameter A with T from equation 2.12] again a progression can be seen, with the under-

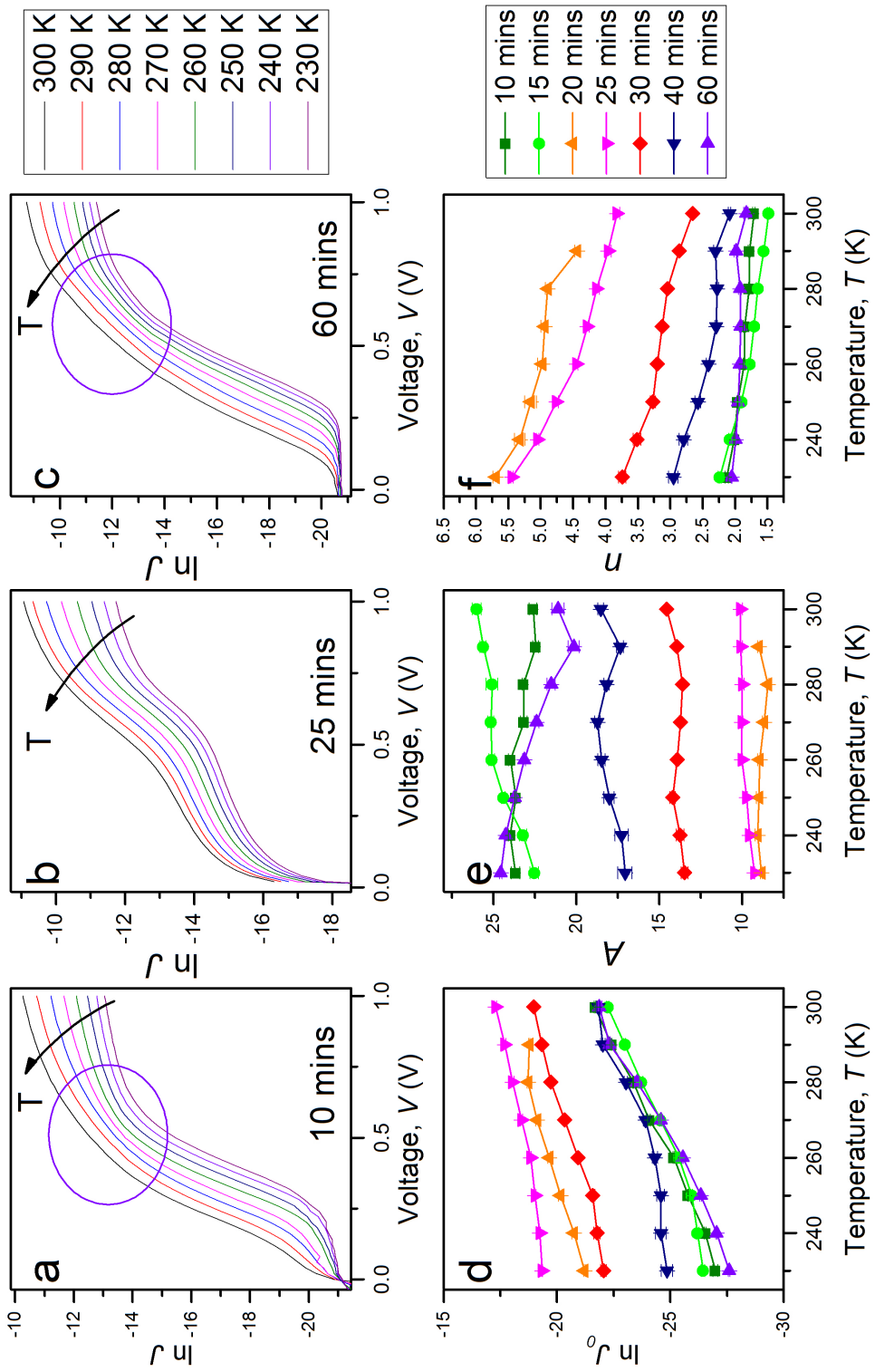

Figure 5.19: Data from $J-V-T$ studies on Series 522 (chloride treated at 410 °C). The upper set of plots demonstrate the three major observed trends described in the text, and show $ln\,J$ for samples a) 522/1 (10 mins), b) 522/4 (25 mins) and c) 515/8 (60 mins). The lower row contains data from all sample cells from Series 522 with the exception of 522/6 (35 mins) which was damaged by the measuring process, and plot temperature dependence of d) $ln\,J_0$, e) A and f) n.

and over-processed samples having room temperature values of A>17, with the more optimised samples showing $A < 15$. Most samples also displayed invariance of A with T, with the exception of the 60 minute sample, where A varied between 20 - 25 over the temperature range displayed. The more optimised samples again demonstrated different behaviour in panel f) [variation of factor n with T from equation B.3], with values of $n > 2$ at all temperatures. Only the under-processed samples showed values of $n < 2$, and all bar the 60 minute sample showed decreasing n with increasing T. The 60 minute sample was invariant across the temperature range with $n \approx 2$.

For the two Series 522 samples seen in figure 5.20 a slightly different pattern was seen: the under-treated sample (30 mins) showed appropriate J_0 behaviour (panel b), invariant A with T (c) and a reducing n with increasing T (d), with $n > 2$. In comparison, the optimised sample (40 mins) showed an unphysical increase of J_0 with decreasing temperature, indicating that the model was not suitable for this sample. When the 40 minute sample was analysed using the single diode model, an appropriate relationship was seen between J_0 and T as can be seen in 5.20 e), and n is seen to reduce with increasing temperature, with a value of $n \approx 1.8$ at room temperature.

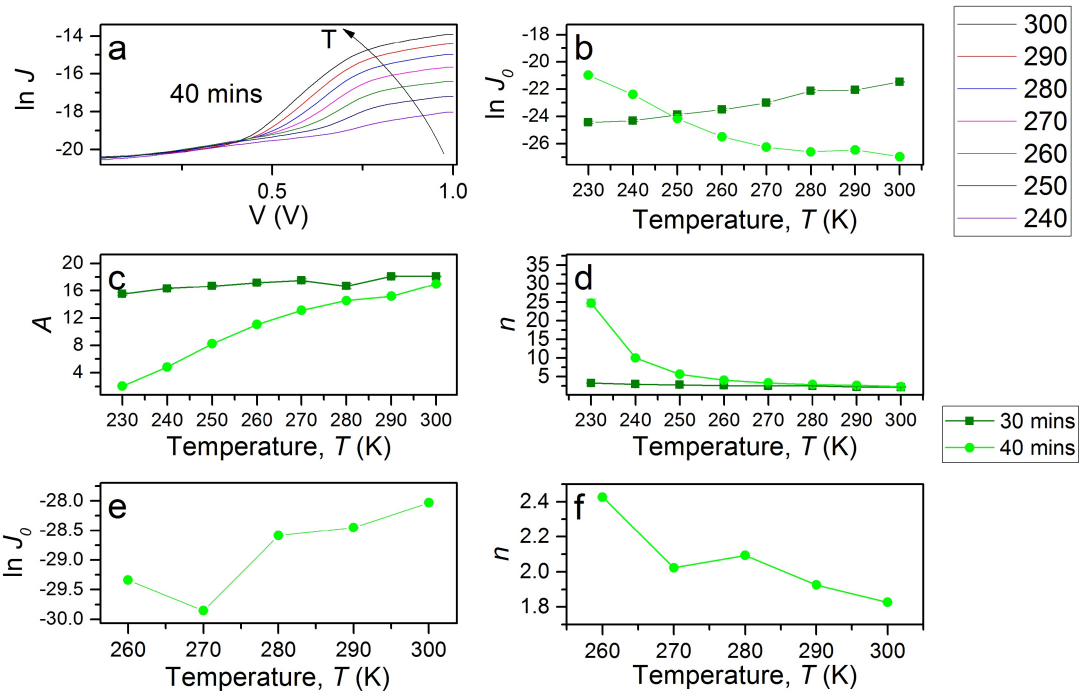

Figure 5.20: JVT data for the Series 522 samples which were chloride processed at 390 °C; a) Raw $J-V-T$ data, analysis using multi-step tunelling model to find b) $ln\, J_0$ vs T, c)A vs T, d) n vs T, and the single diode model to establish e) $ln\, J_0$ vs T, and f) n vs T. The 50 minute sample was damaged during the measuring process so is not included here.

Sample	**Chloride anneal time** (mins)	N_{nA} (10^{14} cm^{-3})	**Forward bias**		**Reverse bias**		
			A 300 K	n 300 K	R 300 K	N_t 300 K (cm^{-3})	$\Delta m/\Delta T$ 250-300 K
522/1	10	0.89	22.6	1.7	1,100	5.3×10^{10}	-9.2×10^{-3}
522/2	15	0.73	26	1.4	1,000	9.5×10^{10}	-2.43×10^{-2}
522/3	20	1.29	-	-	-	-	-3.0×10^{-3}
522/4	25	3.22	10.1	3.8	1,600	7.3×10^{8}	-7.0×10^{-6}
522/5	30	1.39	14.6	2.7	1,700	1.3×10^{9}	-7.5×10^{-5}
522/6	35	2.25	-	-	-	-	-
522/7	40	2.23	18.5	2.1	660	2.7×10^{7}	-1.2×10^{-2}
522/8	60	1.43	N/A	N/A	N/A	N/A	N/A

Table 5.5: The results of analysing $J-V-T$ data for Series 522 (chloride treated at 410 °C) using the multi-step tunnelling model. The table includes calculated values of slope, A, diode factor, n, and number of tunnelling steps R, which are all calculated from the forward bias data. The reverse bias $J-V-T$ data was used to calculate the trap density, N_t and the exponent m. N_{nA} was calculated from $C-V$ analysis and will be discussed in the next section. Calculated errors for all parameters were in the order of 5%. (Data is not available for cells 522/6 (35 mins) or at 300 K for 522/3 (20 mins) through sample breakdown.)

The above trends are now interpreted: for samples processed at 410 °C the data strongly suggest multi-step tunnelling for all samples except the 60 minute sample. Using this model the values for the number of tunnelling steps R, trap density N_t and gradient of m vs T was calculated as shown in table 5.5 (As discussed in the analysis for Series 521, the trap density calculated here is that required for multi-step tunnelling, and is not a measure of the traps present in the sample.) While the gradient m vs T was negative for all tested samples (an indicator of multi-step tunnelling) there appears to be an increase in R in the optimised samples, with a gradual decrease in N_t. For the 60 minute sample a different mechanism is suggested, as parameter A appeared to have a temperature dependence. With this sample appearing to have a constant value of $n = 2$, the data could be consistent with SRH recombination, or recombination in the depletion region. For this sample $ln\, J_0$ was found to be proportional to $1/T$, which is a requirement of the latter mechanism. However, $n\Delta E \neq V_{bi}$, ($V_{bi} = 1.0$ eV, $n\Delta E \approx 2.6$ eV, see section 2.2.3 and equations 2.8, 2.9) making this process unlikely. Without $J-V-T$ under illumination, however, SRH recombination cannot be proved (CdS:O samples were examined in this way in chapter 6). Attempts to fit the data from this sample to a two diode model (Using Orig-

inPro to fit $J1$, $J2$, n_1 n_2, R_{SH} and R_S as free parameters in a similar manner to fitting the single diode equation) also resulted in unphysical results of both n_1 and $n_2 > 2$.

Sample	**Chloride anneal time** (mins)	N_{nA} (10^{14} cm^{-3})	**Forward bias**		**Reverse bias**		
			A 300 K	n 300 K	R 300 K	N_t 300 K (cm^{-3})	$\Delta m/\Delta T$ 250-300 K
522/9	30	1.54	18.1	2.1	1000	3.85×10^{8}	-1.0×10^{-3}
522/10	40	2.17	N/A	N/A	N/A	N/A	4.5×10^{-3}
522/11	50	1.97	-	-	-	-	-

Table 5.6: The results of analysing $J-V-T$ data for Series 522 (chloride treated at 390 °C) using the multi-step tunnelling model. The table includes calculated values of slope, A, diode factor, n, and number of tunnelling steps R, which are all calculated from the forward bias data. The reverse bias $J-V-T$ data was used to calculate the trap density, N_t and the exponent m. N_{nA} was calculated from $C-V$ analysis and will be discussed in the next section. Calculated errors for all parameters are in the order of 5%. (Sample 522/11 (50 mins) unable to be analysed.)

Table 5.6 shows the parameters extracted from analysis of samples processed at 390 °C using the multi-step model. As expected, the 40 minute sample did not fit this model, displaying a positive gradient of m vs T. It is possible this sample had some evidence of recombination in the depletion region, as $n \approx 2$ and $ln\, J_0 \propto -1/T$ [although $n\Delta E \neq V_{bi}$, the extracted values (in this case $V_{bi} = (0.97 \pm 0.01)$ eV, $n\Delta E = (0.79 \pm 0.05)$ eV are of a similar magnitude]. While it is difficult to confirm the exact transport process happening in this sample, it appears clear that it is not the multi-step tunnelling seen in other samples in Series 522.

b) Back contact

Series 522 samples were analysed in the same fashion as for Series 521 using the method outline in section 3.2.3 using $J-V-T$ data. As before the selection of the model chosen to extract R_S was made on the goodness of fit to the model to the data, and the fit equation chosen to produce a high quality fit. The results are shown in table 5.7 for the 410 °C samples and table 5.8 for the 390 °C samples.

The values for ϕ_b seen in table 5.7 started at 0.43 eV in the 10 minute sample, before dropping to $\gtrsim 0.25$ eV for the remainder of the series, with the exception of the 30 minute sample. This plate showed a slightly higher value of 0.32 eV. In figure 5.8 the optimised 40 minute sample also showed a higher value of 0.32 eV

Sample	**Chloride anneal time**	R_s **calculation**	ϕ_b eV	**Fit equation**
522/1	10	Single diode	0.43 ± 0.04	5.1
522/2	15	Slope	0.250 ± 0.006	5.1
522/3	20	Slope	0.265 ± 0.006	5.1
522/4	25	Slope	0.245 ± 0.018	3.3
522/5	30	Slope	0.322 ± 0.005	5.1
522/6	35	-	-	-
522/7	40	Slope	0.270 ± 0.006	3.3
522/8	60	Single diode	0.26 ± 0.06	3.3

Table 5.7: The calculated values for the back contact barrier height ϕ_b for Series 522 processed at 410 °C, with the equations used to calculate R_S and ϕ_b (where 'slope' refers to the method in section 3.2.3 and 'single diode' refers to equation 3.4). In each case the equation chosen produced the best fit as measured through χ^2 and adjusted R^2.

(albeit with high error), a significant change from the 30 minute sample with a low 0.22 eV value.

The values seen for ϕ_b are on the low side of normal for CdTe cells. In particular, while the value of 0.43 eV (522/1, 410 °C 10 mins) was comparable to literature values, those for samples treated for longer times, or at 390 °C were all in the range 0.245 - 0.35, which is low compared to most published values for Au/CdTe contacts. The explanation of this may lie in the shapes of the $J-V$ curves (figure 5.17) which have slight kinks in the forward bias regions, and show no signs of the usual back contact rollover. Therefore it is likely that the devices are not described by the usual two-diode model. Indeed it has been speculated

Sample	**Chloride anneal time**	R_s **calculation**	ϕ_b eV	**Fit equation**
522/9	30	Slope	0.216 ± 0.013	5.1
522/10	40	Single diode	0.35 ± 0.07	5.1
522/11	50	-	-	-

Table 5.8: The calculated values for the back contact barrier height, ϕ_b for Series 522 processed at 390 °C, with the equation used to calculate R_S (where 'slope' refers to the method in section 3.2.3 and 'single diode' refers to equation 3.4), and which equation was used to calculate ϕ_b. In each case the equation chosen produced the best fit as measured through χ^2 and adjusted R^2.

that CdS:O segregates into CdS and CdS:O compositions introducing a further electrically active interface. This would make analysis using the methods used here inappropriate. Hence the barrier heights represented in tables 5.7 and 5.8 should be treated with caution.

5.3.2.3 Shallow and deep levels

a) Shallow levels

$C-V$ analysis was used to determine shallow doping levels in the same manner as for Series 521 (detailed in section 3.3.2.). The results from this analysis can be seen in figures 5.21 (for samples treated at 410 °C) and 5.22 (for samples treated at 390 °C).

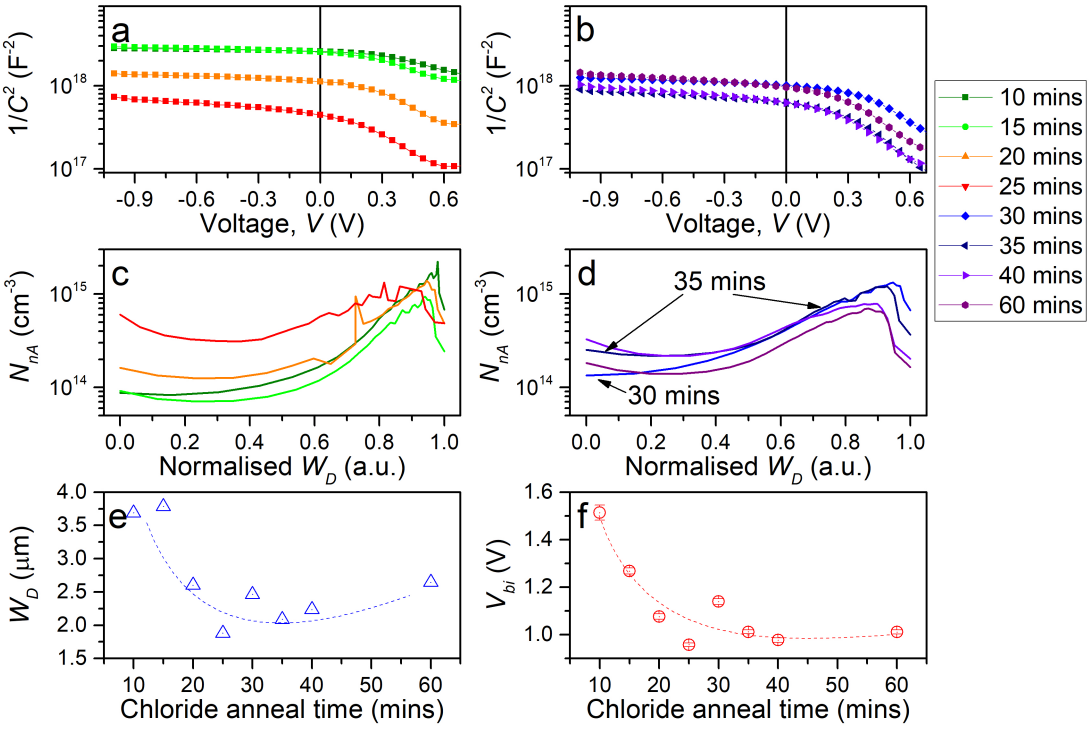

Figure 5.21: Data from $C-V$ analysis of Series 522 ($MgCl_2$ annealed at 410 °C); Mott-Schottky plots for a) 10 - 25 minutes, and b) 30 - 60 minutes, depth density plots (N_{nA} vs normalised W_D) for c) 10 - 25 minutes, and d) 30 - 60 minutes, e) depletion width W_D vs treatment time, and f) built-in voltage V_{bi} vs treatment time. The broken lines are guides to the eye.

The Mott-Schottky plots seen in figure 5.21 a) and b) show the changing junction capacitance as a function of treatment time, with the neutral-bias capacitance increasing from ~0.6 nF ($C^{-2} \approx 3 \times 10^{18}\,F^{-2}$) at 10 minutes of treatment to ~1.5 nF ($C^{-2} \approx 4 \times 10^{17}\,F^{-2}$) at 25 minutes. Longer treatment times cause

the capacitance to decrease slightly to ~1 nF ($C^{-2} \gtrsim 7 \times 10^{17}\,\mathrm{F}^{-2}$). The forward bias curve shape can also be seen to change slightly with chloride processing, as the change of capacitance over the $p-n$ junction (visible at voltages $\gtrsim 0.3\,\mathrm{V}$) was greater in the samples processed for > 25 minutes. Most of the curves have not quite plateaued to zero slope in reverse bias, with the exception of the 10 minute sample. The anomalous 30 minute sample (section 5.3.2.1) had a gradient more comparable to the 10 minute sample than to its nearest neighbours in time, a feature which was reflected in the depth density plots (figure 5.21 c) and d). Both the 10 and 30 minute samples showed a large variation of doping density across the sample, steadily increasing from $< 1 \times 10^{14}\,\mathrm{cm}^{-3}$ to $> 1 \times 10^{15}\,\mathrm{cm}^{-3}$. All the other samples showed the characteristic 'U' shape, with the full width doping values highest across the 25 minute sample. The depletion width W_D is shown in figure 5.21 e) and can be seen to decrease from $> 3\,\mu\mathrm{m}$ in the under treated samples to $\lesssim 2\,\mu\mathrm{m}$ in more optimised samples, before rising again to $> 2.5\,\mu\mathrm{m}$ by 60 minutes. The 30 minute sample is as before thought to be a bad data point. A similar change can be seen in the built-in voltage V_{bi}, with a value of $\approx 1.5\,\mathrm{V}$ in the as-grown sample, rapidly dropping to $< 1.1\,\mathrm{V}$ by 20 minutes.

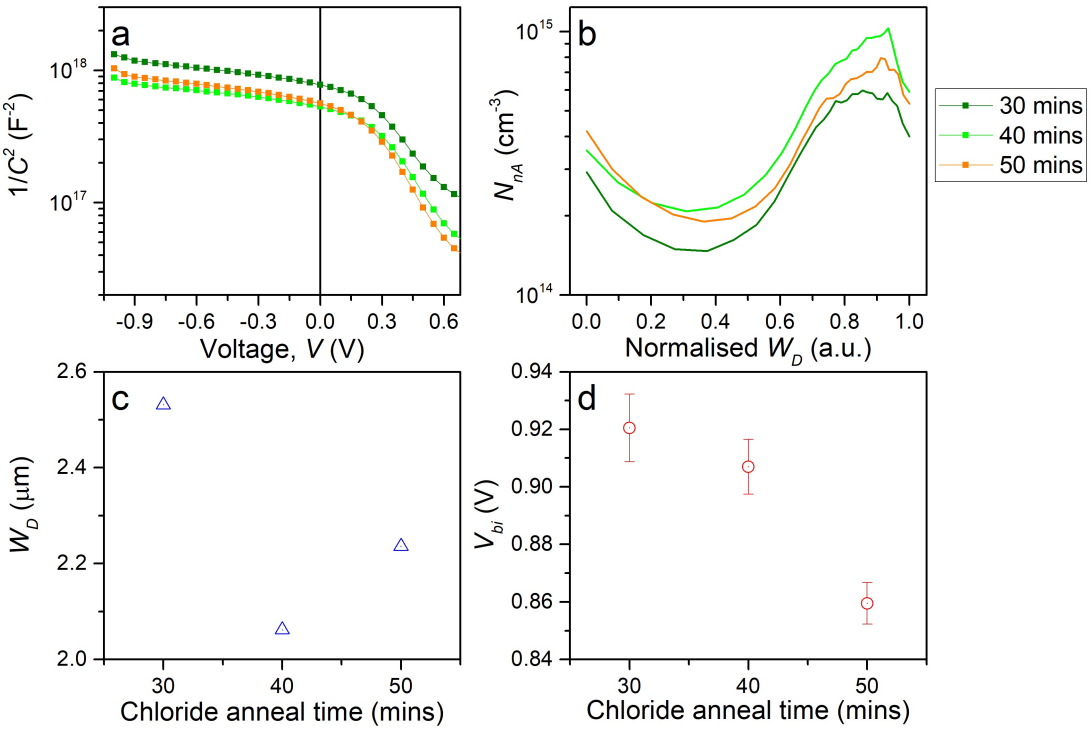

Figure 5.22: $C-V$ data for Series 522 $MgCl_2$ annealed at 390 °C; a) Mott-Schottky plots, b) doping density profile, c) W_D vs treatment time, an d) V_{bi} vs treatment time. The 40 minute sample had the highest shallow doping levels.

Many similar trends are seen in the data from Series 522 samples processed

at 390 °C as seen in figure 5.22. Subtle changes in the gradient of the forward bias Mott-Schottky plots (a) correspond to different minimum values in the depth density plot, with the 40 minute sample displaying the highest doping across the cell. A minimum in W_D was seen in the 40 minute sample at $\approx 2.1\,\mu m$ (figure 5.22 c), but unlike the 410 °C samples, the V_{bi} did not have a similar minimum, dropping instead to $\approx 0.86\,V$ by 50 minutes of treatment.

The $C-V$ data for Series 522 is now interpreted. The Mott-Schottky plots in figures 5.21 a), b) and 5.22 a) all have the shape commonly seen in CdTe devices. Aside from the 410 °C 10 minute sample, all plots demonstrate a non-zero gradient at the extremes of negative bias, which implies incomplete depletion of the space charge region (the 10 minute sample has appearances consistent with full depletion). The changing gradients with bias is indicative of non-homogeneous doping across the cell, as shown in the depth density plots [figures 5.21 c), d) 5.22 b)]. The more optimised cells treated at 410 °C (namely the 25 and 35 minute samples) had the highest values of N_{nA}, and are the most consistently doped as a function of depletion width. A progressive improvement in doping with treatment time could be seen in these three plots, with a decline in doping levels with over-treatment. It is possible the minima in depletion widths seen in figures 5.21 e) and 5.22 c) may signify improved quality of the $p-n$ junction with more abruptly defined borders. The physics behind the changes in V_{bi} is not clear. (Assessment of V_{bi} in similar cells under illumination is discussed in chapter 6.3.1.2)

b) Deep levels

Thermal admittance spectroscopy (TAS) was used to study deep trap levels in Series 522. The results are shown in figure 5.23 for the samples processed at 410 °C and figure 5.24 for those processed at 390 °C.

Figure 5.23 a) shows the trap energies recorded as a function of the $MgCl_2$ treatment time. Some treatment times generated multiple trap signatures (20 and 25 minutes) whereas the others generated only one. Though the data is rather scattered it is significant that although the best performing cells did not have the shallowest traps, the other devices all had deeper traps. Hence all of the other cells may be expected to suffer greater recombination losses. This behaviour is similar to that shown for the CdS window layer samples in Series 521 (section 5.3.1.3). This will be discussed in section 5.4.

Figures 5.23 b) and c) show the cross section σ_{nA} and trap density N_{nt} respectively. The cross section behaved in a similar manner to that seen in the previous series, with a reduction to minimum values in the optimised samples. In contrast with Series 521, the trap density appeared to peak with the more optimised samples to a maximum of $\approx 2 \times 10^{14}\,cm^{-3}$ in the 25 minute sample. In

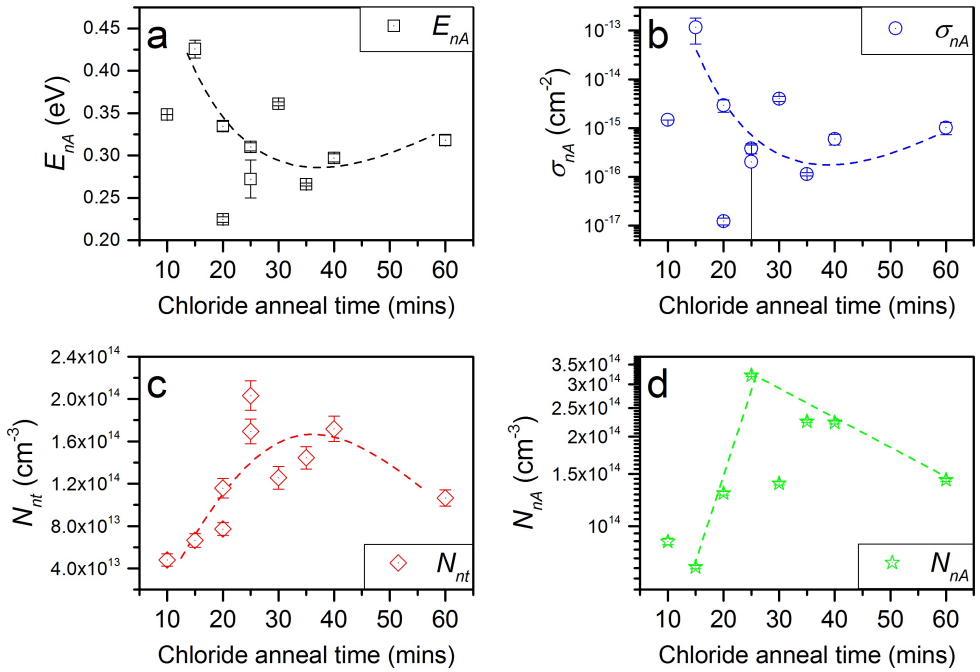

Figure 5.23: Apparent trap data of Series 522 (annealed at 410 °C) analysed at 0 V bias; a) E_{nA} b) σ_{nA}, c) N_t, and d) N_{nA}. Samples processed for 20 and 25 minutes show a pair of trap energies (and therefore densities and cross sections) whereas all other samples show only one. The dotted lines are guides at the eye showing the general trends, see text.

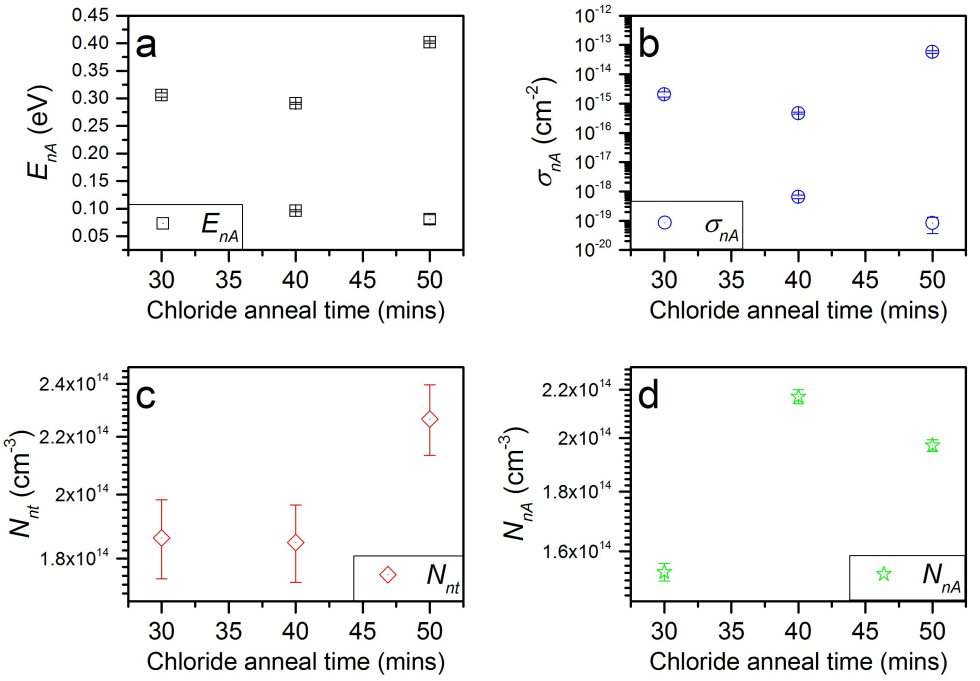

Figure 5.24: Apparent trap data of Series 522 (annealed at 390 °C) analysed at 0 V bias; a) trap energies, b) capture cross sections, c) deep level densities, and d) shallow doping densities.

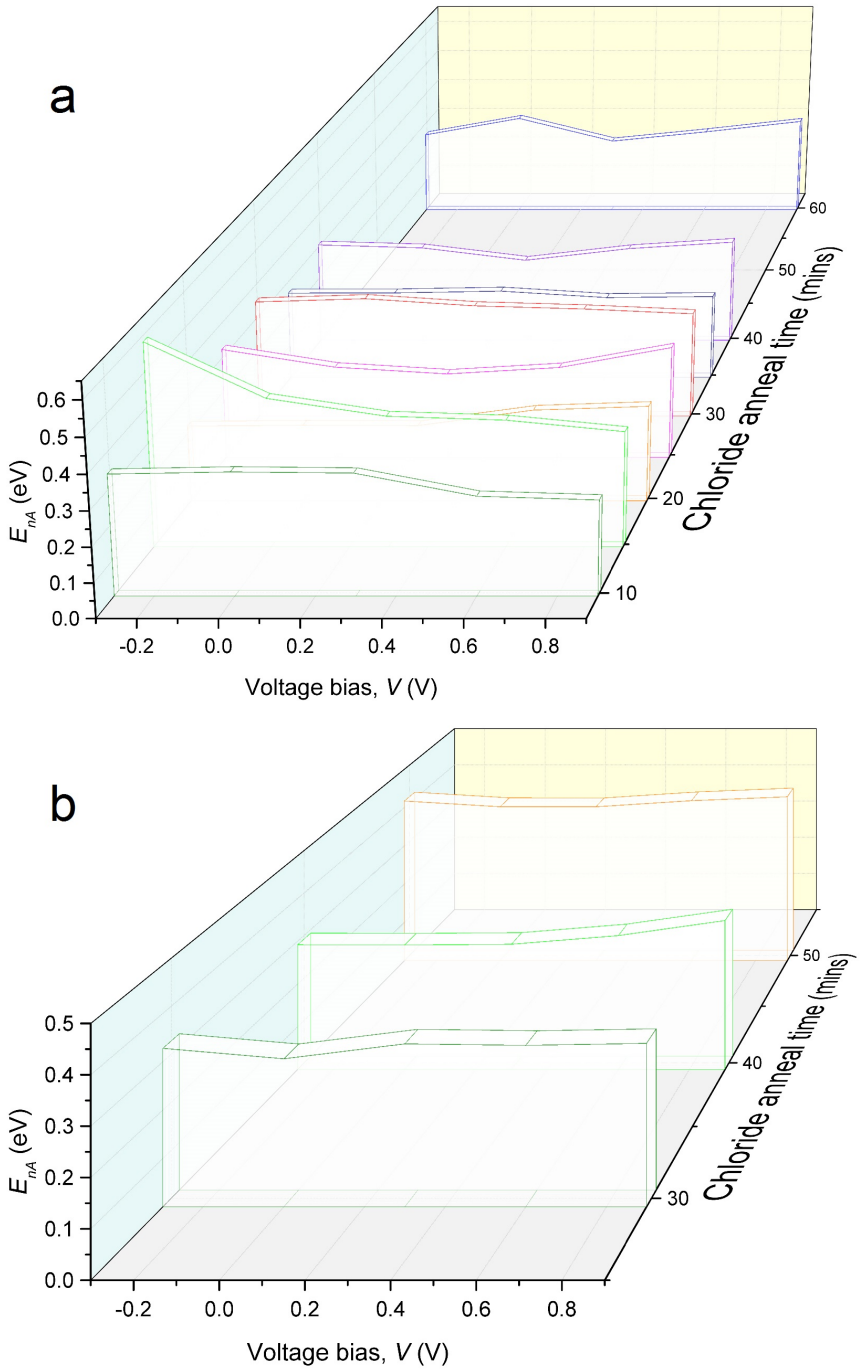

Figure 5.25: Trap energies E_{nA} as a function of voltage bias and $MgCl_2$ treatment time for Series 522 processed at a) 410 °C, and b) 390 °C.

figure 5.23 d) the minimum shallow doping level is shown, which can be seen to have increased to a maximum between 25 - 40 minutes before decreasing again.

The samples processed at 390 °C (figure 5.24) show similar trends in the data, with the exception of N_{nt} which was seen to decrease slightly in the optimised sample, (i.e. similar to that in Series 521). Again the trap energies were the lowest in the optimised sample (a), with two traps evident at energies of (0.0962±

0.0018) eV and (0.2911 ± 0.0016) eV in the 40 minute sample. The capture cross sections (seen in panel b) were at a minimum in the 40 minute sample, with the < 0.10 eV traps having smaller cross sections ($< 1 \times 10^{-18}\,\mathrm{cm}^{-2}$). This sample also demonstrated the highest shallow doping (figure 5.24 b) at $(2.17 \pm 0.03) \times 10^{14}\,\mathrm{cm}^{-3}$.

These results are now discussed. For both processing temperatures, a change was seen in trap parameters as a function of $MgCl_2$ treatment time. The most optimised devices (25 and 35 minutes samples treated at 410 °C, and 40 minute sample treated at 390 °C) combined the lowest trap energies with highest shallow doping and low capture cross sections. The impact on trap density is not consistent between the two treatment temperatures. In several of the samples the trap energy fluctuated between 0.25 - 0.35 eV depending on bias. This can be seen in figure 5.25 a), which shows E_{nA} as a function of both treatment time and DC bias. This is particularly evident in the samples treated for 10, 40 and 60 minutes. It is speculated that in this series there were several traps present in the 0.25 - 0.35 eV range, with the most influential trap dominating the TAS spectrum.

5.3.2.4 Equivalent circuit

Impedance data from the Series 522 samples was analysed to find most appropriate equivalent circuits. The circuit models considered are shown in figure 4.3. As with Series 521 models 'h' and 'i' were not included in the following analysis, as good quality fits for these models resulted in unphysical circuit components. The fit quality to the other models at 0, 0.3 and 0.6 V are shown in table 5.9. For both treatment temperatures it is possible to see a reduction in appropriate circuits with increasing forward bias, with fewer and poorer quality fits evident at 0.6 V. For all Series 521 samples the turn-on voltage was < 0.5 V, with the voltage range 0.5 - 0.8 V showing a slight kink for many of the 410 °C processed devices. Circuit 'c' was found to provide the highest quality fits for both temperature ranges in the voltage range 0 - 0.3 V, but at 0.6 V was often impossible to fit without unphysical CPE^P values of > 1. For the latter voltage range, circuit 'b' was used.

Values of the series resistance R_S calculated from the fitted circuit are shown in figure 5.26. In figure 5.26 a) the value starts at a comparatively low level of $< 200\,\Omega$ in the 10 minute sample (410 °C) before reaching a maximum of $> 200\,\Omega$ at 15 minutes of treatment. Following this there is a gradual reduction to a minimum of $< 30\,\Omega$ at 35 minutes, before a further increase. Figure 5.26 b) shows a similar trend, with a rapid decrease in R_S from $\sim 200\,\Omega$ to $< 40\,\Omega$ between 30

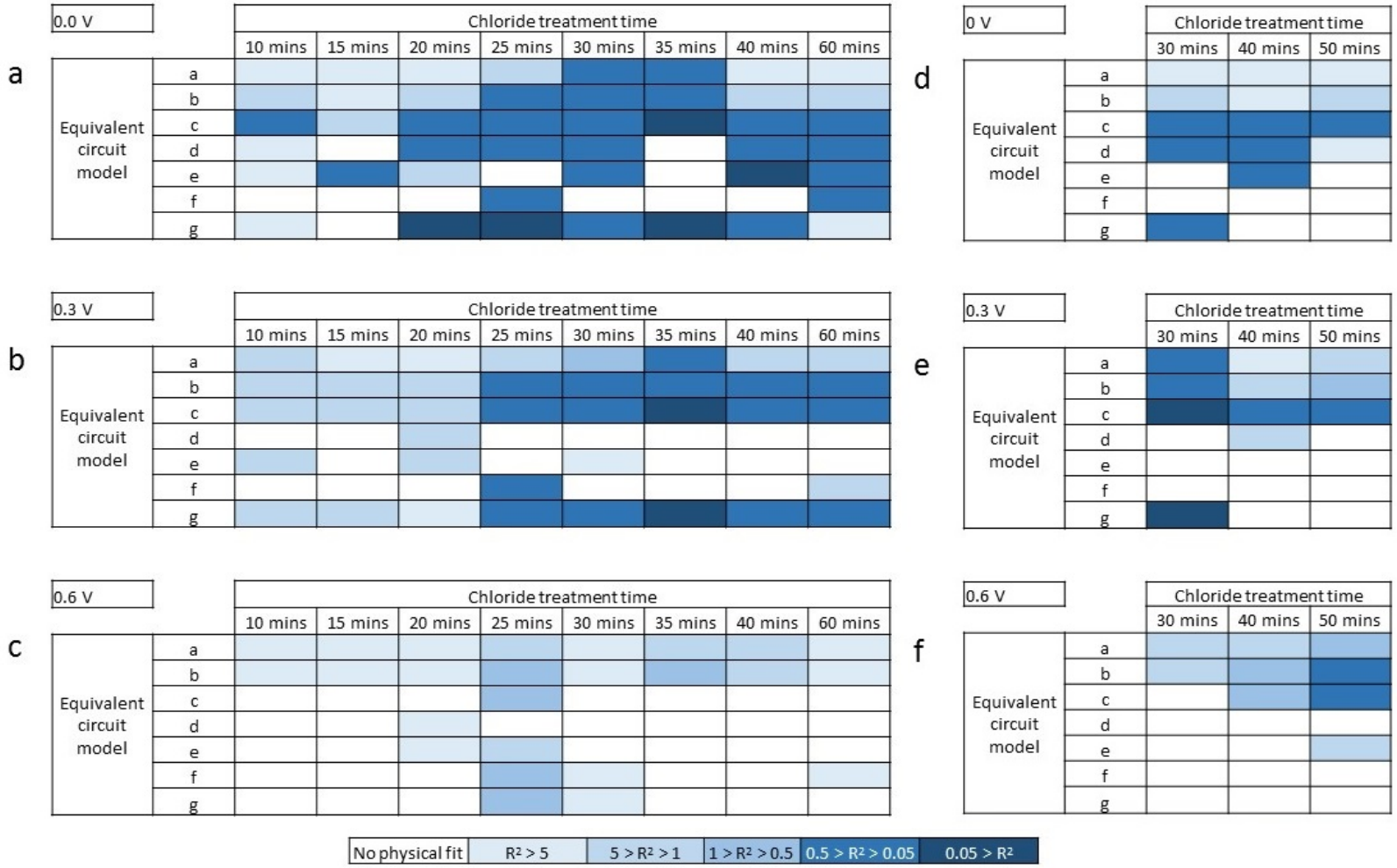

Table 5.9: A schematic to show the range of fit quality for equivalent circuit models a - g (see figure 4.3) to admittance data at a) 0 V, b) 0.3 V and c) 0.6 V for Series 522 processed at 410 °C, and at d) 0 V, e) 0.3 V and f) 0.6 V for Series 522 processed at 390 °C. The fit quality is indicated by a colour guide corresponding to the sum of the squares between the data and the fit. Fits which do not converge, or provide unphysical circuit components are shown in white.

and 40 minutes of treatment, before a slight increase.

The above equivalent circuit results are now discussed. It has previously been noted that several of the samples in Series 522 did not appear to be modelled correctly by a two diode model. This appears to be the case on more detailed analysis, with no high-quality ($0.05 > R^2$) two diode model fits, and only two high quality R_S, $R-C$, $R-CPE$ models (model 'c'). Better quality fits were achievable with more complicated circuits, especially model 'g', but only for the more optimised samples with less evident 'kinks' in the $J-V$ curves. There are no high quality fits for the under- and over-processed samples for the samples processed at 410 °C. This suggests that none of the varied equivalent models a - i studied here fully describe these Series 522 samples. This appears to be related to the CdS:O layer, and raises the possibility again of a further electrically active junction being present which cannot be adequately described using the models here.

For the models 'b' and 'c', which were the closest approximations to the effective circuits for these samples, the data suggested that there was an initial increase in R_S in under-processed samples, and that optimisation results in a local minimum value for series resistance. This is discussed later in the thesis.

5.3.2.5 Summary of results for Series 522

The following statements summarise the results from analysis of Series 522 (i.e. cells with CdS:O window layers).

- Progressing treatment with $MgCl_2$ lead to a peak in performance. The highest efficiency devices combined a peak in V_{OC} with a high J_{SC} and FF. Over-treatment lead to a decline in V_{OC}, but little effect on J_{SC} or FF.

- Issues with sample consistency and reproducibility lead to some sample plates not performing as expected, and the presence of slight 'kinks' in the $J-V$ curves of under-and over-processed samples, limiting their interpretive value. This inconsistency also generated scatter in the trends for deep and shallow level behaviour.

- The highest performing cells combined the highest shallow doping levels with the lowest trap energies and capture cross sections. They also had the lowest values for R_S.

- EQE demonstrated an increased window layer band gap compared to cells with a CdS window layer, and increased absorption across the shorter wavelength region. This plateaued after treatment optimisation.

- Current transport showed evidence for multi-step tunnelling for all devices with two exceptions: the optimised 40 minute sample treated at 390 °C showed some evidence for recombination in the depletion region, while the limited data for an over-processed device heated for 60 minutes at 410 °C sample suggested SRH recombination (the optimised 35 minute sample treated at 410 °C, and over-processed 50 minutes sample treated at 390 °C were unable to be analysed).

- The best fitting equivalent circuit model was circuit 'c', a series resistance with an $R-C$ and an $R-CPE$ element in series. The CPE was capacitive in nature.

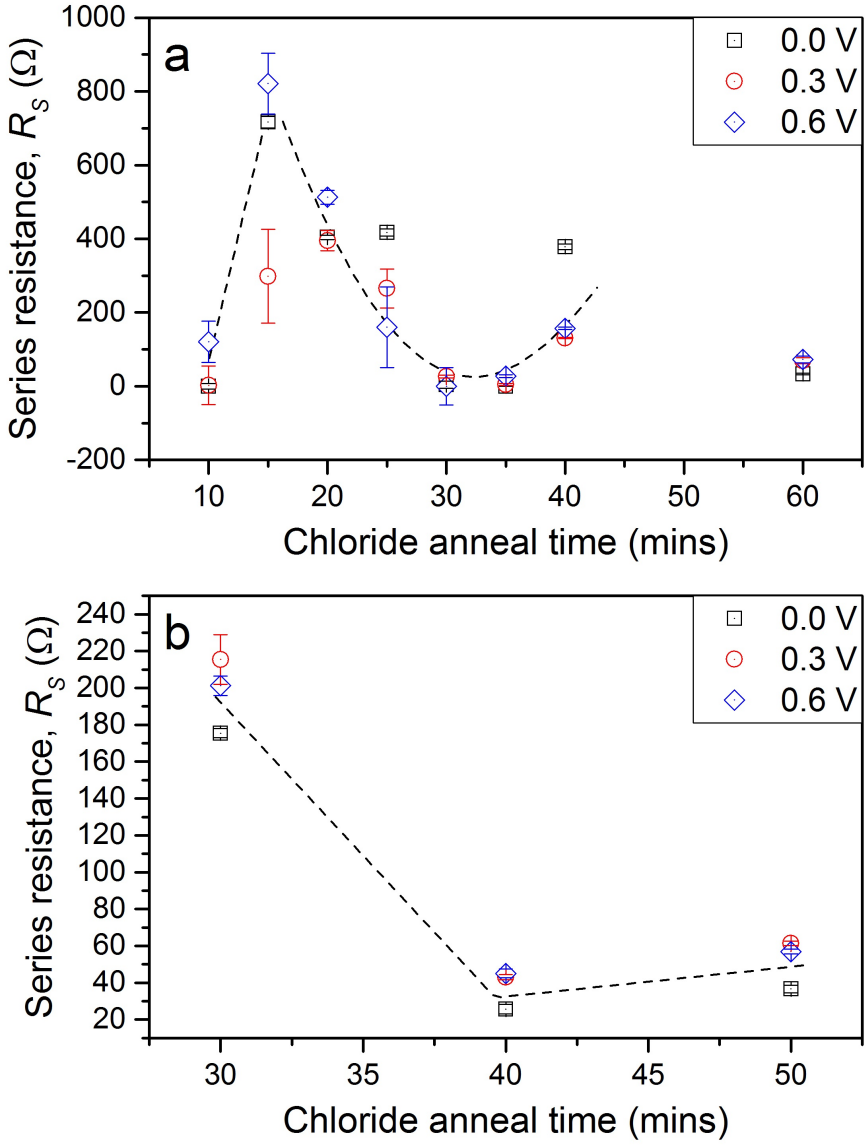

Figure 5.26: Variation in the values of series resistance with chloride annealing time obtained from impedance analysis data using circuit 'c' from figure 4.3 at 0 - 0.3 V and 'b' at 0.6 V. Samples processed at a) 410 °C, and b) 390 °C.

5.4 Discussion

The findings from analysis of Series 521 and 522 are now discussed. The two sample sets were designed both to compare the differences arising from the use of CdS and CdS:O window layers and to expand the number of data points for deep and shallow level evaluation. Although the CdS:O series (522) showed some scatter and a bad data point, nevertheless the data sets share some overall trends which are highlighted in the following discussion.

Unfortunately Series 522 suffered from reproducibility issues, which is a recognised problem with CdS:O window layers. The $J-V$ shape in this series showed a slight kink, therefore the two diode model was not able to adequately describe the cell function. As consequences of this, some consistency problems were evident across the data set, and lower values of ϕ_b than expected were generated from series resistance measurement. Attempts to corroborate and expand the data set for CdS samples as started in Series 521 were therefore frustrated and so the discussion focuses on overall trends. In the following discussion sample 522/6, the 30 minute sample processed at 410 °C, is taken to be a rogue data point and is not considered further.

a) Performance

In both series or cells there was a trend of rapid improvement in device performance followed by gradual decline related to the duration of $MgCl_2$ treatment. Series 521 cells reached a higher efficiency than those in 522 with less variation in parameters between contact dots on the same sample plate. The peak in performance in Series 521 resulted largely from a maximum in J_{SC} and FF, with a shallow maximum in V_{OC}. In contrast Series 522 demonstrated an increasing J_{SC} to a plateau level, which lead to a maximum efficiency when combined with a peak in V_{OC}. The voltages were in general lower in the latter series however, resulting in lower overall efficiency. Despite similar maximum values for J_{SC} it was seen in EQE that Series 522 had an increased wavelength range of absorption, with the band gap of the window layer shifted to higher energies. It can also be seen from the EQE below 500 nm that for all of the cells in 521 the optical losses in the CdS were large, due to the thick CdS used to reduce shunting [28]. This area showed an increase in EQE in Series 522 samples which is a recognised change associated with CdS:O. It is thought to be caused by the presence of CdS:O creating a softer junction between the window layer and the CdTe resulting in a range of band gaps [27]. The junction position also appeared to be improved in Series 522 as indicated by the squarer region above 550 - 850 nm in figure 5.18 [1].

The EQE differences between Series 521 and 522 were related to the presence

of CdS:O. With its increased band gap it allowed passage of higher energy photons into the devices. The metallurgical junction between the CdS:O and CdTe is also reported to be smeared, thought to be indicative of a graded band gap variation with different alloys across the junction. It is likely that there was some breakdown of the CdS:O into CdS and CdS:O here, which acted as a further electrically active layer within the cell. Compared to Series 521, the V_{OC} was lower in Series 522 devices processed at 410 °C, and higher in those treated at 390 °C. This may be indicative of an improved junction at the lower temperatures, with fewer voltage reducing electrically active defects. It is possible to see evidence for this in the $J-V$ curves, with that of Series 522 treated at 390 °C for 40 minutes (figure 5.17 b) demonstrating the most ideal curve of both series, with neither roll-over nor 'kink' visible in this optimised sample.

b) Current transport ($J-V-T$ analysis)

The dominant current transport method seen in both Series 521 and 522 was multi-step tunnelling, with a few notable exceptions. The most optimised samples of both series demonstrated anomalous $J-V-T$ behaviour, which for Series 521 did not fit to a physical model. For sample 522/10 (treated at 390 °C for 40 minutes) evidence was found to suggest recombination in the depletion region. This transport mechanism is mediated by the minority carriers, rather than the majority carriers involved in multi-step tunnelling [29, 30]. Such a change in behaviour could be indicative of a reduction of the influence of trap states in the optimised sample, through reduced cross section and trap density. As the multi-step tunnelling mechanism assumes a uniform trap distribution (in energy) as opposed to localised mid-band-gap levels for recombination in the depletion region, this transport change may indicate a change in distribution. It is possible that the spectrum of trap levels present in these samples had become narrowed into more distinct regions, separated by regions without trap states in between, such that tunnelling was no longer energetically favourable. Similar conversion from tunnelling to depletion region recombination has been observed as a function of $CdCl_2$ treatment in CdTe device [31]. Many other studies have found multi-step tunnelling in as-grown and $CdCl_2$ treated cells, often changing to a different mechanism at typical working temperatures [2, 4, 5, 32, 33]. In both $CdCl_2$ and $MgCl_2$ treated samples evidence of both mechanisms was present at different temperatures [34].

c) Shallow and deep levels

In both Series 521 and 522, the best performing devices had among the highest levels of shallow doping of each set and over-treatment with $MgCl_2$ reduced the

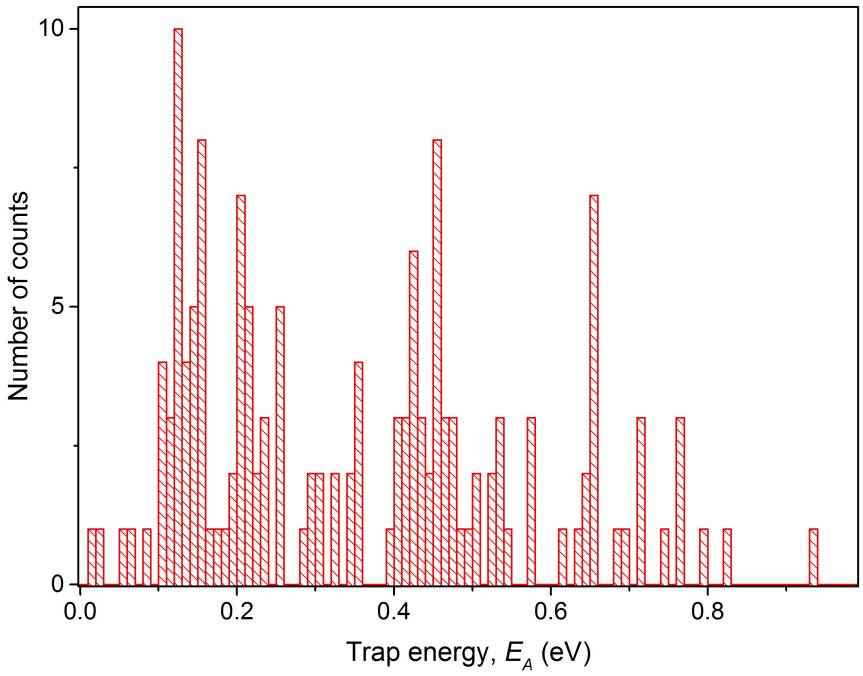

Figure 5.27: A histogram to show the examples of spread of experimental and theoretical trap levels reported in CdTe and CdTe solar cells [16, 21, 22, 36–45].

apparent doping. The values for N_{nA} were in the range $(0.9\text{-}3.0)\times10^{14}\text{cm}^{-3}$ which are consistent with values for $CdCl_2$ treated cells in the available literature [9,20]. As a comparison, 13.0% and 14.8% efficient cells produced by Major *et al* and processed with $CdCl_2$ were reported to have doping levels of $\sim 3.5 \times 10^{14}\,\text{cm}^{-3}$ and $\sim 1.5 \times 10^{15}\,\text{cm}^{-3}$ respectively [1,35].

Deep trap behaviour appeared significantly altered as a function of chloride processing time across both series. Rather than demonstrating sets of discrete energy levels as expected, the TAS analysis has shown continuous variation in E_{nA}, with an almost linear decrease in Series 521 from 5 minutes until optimisation was reached (at 25 minutes in this series). This decrease was also replicated in trap density and cross section. At the point of highest PV performance there was a minimum in the trap energies, densities and cross sections for both Series 521 and 522. Beyond this point all three parameters started to increase again. In both series, over-treatment with chloride corresponded with a shift back towards higher trap energies, cross sections and densities (however the trap density for Series 522 devices processed at 410 °C behaved anomalously and appeared to show a maximum rather than a minimum for the highest performing devices). It appears that a saturation point is reached, beyond which the presence of chloride acts to create more recombination and reduce cell performance.

According to current understanding of traps, specific chemical vacancies, substitutions and interstitials are associated with very specific energy values. The

histogram in figure 5.27 shows a selection of theoretical and experimentally determined trap levels reported in CdTe, some of which have been identified with specific chemical complexes. As an example, the so-called 'A-centre' is generally accepted to be the (V_{Cd} + Cl_{Te}) defect with a binding energy of $\sim 0.14\,eV$, although there are several other explanations as to the precise nature of the defect [46–52]. Indeed, there is considerable evidence of the specific chemical nature of this defect using techniques such as optically detected magnetic resonance (ODMR), electron paramagnetic resonance (EPR) and photo-luminescence (PL) used to characterise these defects [53]. It can be seen from the above figure that there are reports of, or predictions for, traps in almost every energy range between the valence band maximum and the mid-gap position. Generally in the literature the presence of a trap of a particular energy is therefore considered to be evidence of specific chemical complexes present in the devices. However, in this chapter it has been shown that the trap parameters vary significantly as a function of chloride treatment time, and a single 'snapshot' of trap levels in an optimised device may be oversimplifying the underlying physical processes.

The levels in this work are not thought to demonstrate changes from one chemical complex to another, as this structural change would be unlikely to present in the manner seen here, with an almost continuum of trap energies rather than hopping from one discrete state to another. There are three other likely explanations for this observed behaviour.

(i) There is a 'ladder' of closely adjacent energy states caused by chemical complexes, dangling bonds and structural defects, the activation energy of which is slightly modified by the local lattice. Annealing in the presence of a chloride changes the relative concentrations of these complexes, such that under TAS the AC fluctuation is sufficient to sample several different traps but not resolve them, creating a subsequent trap signature as a composite of several trap characteristics.

(ii) Grain boundaries (GBs) interact with discrete trap centres, and modification of the grain boundary potential creates a spectrum of apparent trap energies.

(iii) The traps observed are measurements of the GB potential itself, and that this potential is continually modified by chloride annealing.

It is hypothesised that the latter of these explanations is the most promising. Lourenço *et al* used DLTS to find a similar gradual reduction in trap energies with increasing $CdCl_2$ application, with unusually high capture cross sections [54].

They speculated that the measured defects were situated in, or related to the valence band deformation associated with the GBs. There is considerable evidence of GB modification with annealing and/or chloride treatment. Theoretical studies have predicted that Cl^- and $Cu_2{}^+$ ions can passivate grain boundary defects; Te defects are more easily passivated than Cd cores, but can not be completely passivated through these two ions, and although Cd cores are more difficult to passivate, they are less detrimental to carrier transport [55]. An atomistic approach has also shown that sufficient Cl atoms should segregate into GBs in high enough concentration to invert them to n-type, creating local fields which enhance collection [56] (i.e. downward band bending, see figure 5.28 a). Experimental studies have also shown supporting evidence; annealing has been shown to reduce stacking faults, shallow defects and surface roughness [57], and $CdCl_2$ treatment increases grain growth and recrystallisation [58,59]. The action of both these effects would be to reduce the GB surface area per volume of thin film. GBs in under-treated devices have been demonstrated to be strong sites for carrier recombination, yet after $CdCl_2$ treatment they become highly efficient current collectors associated with a high density of Cl at the grain boundaries [60, 61]. Scanning Kelvin probe measurements on As-doped devices showed evidence of *upward* band bending at GBs [62] (figure 5.28). Over-annealing, either at over-optimal temperatures or longer times, increase Cl at the CdS/CdTe interface, associated with a deterioration in cell performance [63].

The data in this chapter would support two chloride mechanisms acting in opposition. Firstly, a positive effect arising from local GB field modification, leading to increased charge collection, and secondly, over-treatment causing accumulation of chloride at the CdS/CdTe interface, increasing series resistance. The annealing in combination with the chloride is thought to act to improve the crystal structure, reducing structural defects and therefore improving carrier lifetime. Segregation of the chloride to grain boundaries may act to allow dopant atoms trapped at these interfaces to contribute to doping [64, 65]. The reducing nature of the trap energies may suggest an upward band bending at the grain boundaries with chloride optimisation, such as seen in figure 5.28 b), as TAS samples traps which cross the Fermi level, and it is difficult to envision how a $p-n-p$ GB would or could produce the observed TAS results.

The impact of the cation used in the chloride treatment compound is not entirely clear. There are certainly differences in performance from the use of other chlorides (e.g. NH_4Cl, KCl, MnCl), but the general trends seen in this chapter are similar to those reported elsewhere for $CdCl_2$ treatment [11, 35, 54].

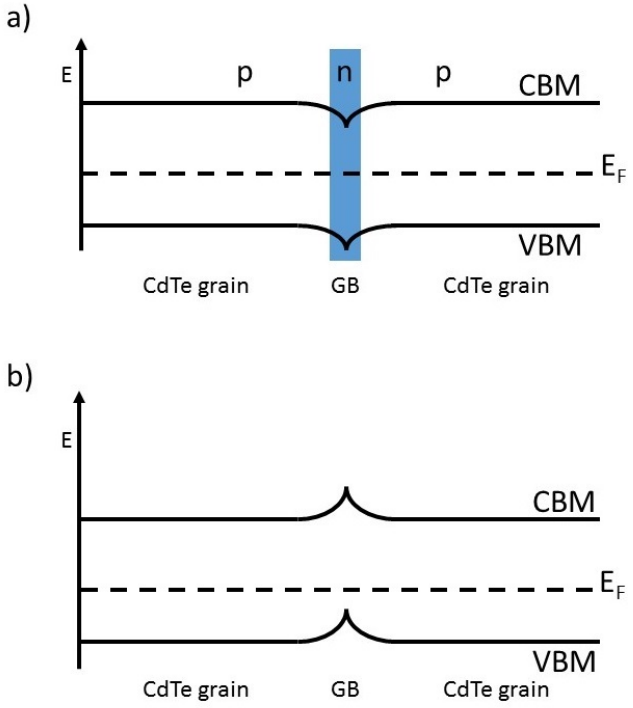

Figure 5.28: Schematics to show the band bending at a grain boundary (GB) between two CdTe crystals, with a) downward band bending leading to type inversion, and b) upward band bending.

d) Equivalent circuits

It was possible to model data from both series of cells to circuit model 'c' which consists of an $R-C$ component, thought to represent the main junction, in series with an $R-CPE$ segment, likely to be a distribution of grain boundaries and various chemical traps, and a series resistance. For Series 522 the CPE was better modelled as a capacitor at high forward bias (i.e. $CPE^P = 1$). More complicated circuits with discrete traps in parallel could not be made to work. For all the devices in both series, the value of CPE^P was between 0.9 and 1, which can be associated with inhomogeneities causing a double-layer capacitance, and indeed has been noted in equivalent circuit analysis of $CdCl_2$ processed CdS/CdTe cells before [7].

For both series it was found that the AC and DC series resistance changed as a function of treatment time, with local maxima in under-processed samples and local minima at optimisation, before rising again slightly. The reduction to minimum levels could be related to the local maximum in shallow doping.

5.5 Implications for improving cell performance

The experiments discussed in this chapter have demonstrated that activation of CdTe solar cell devices with $MgCl_2$ produces similar effects on the electronic properties as activation with $CdCl_2$ does. This is further evidence that could support the replacement of the industry standard $CdCl_2$ in favour of the cheaper and non-toxic $MgCl_2$. It also appears that a peak in performance is achieved with an optimal treatment with $MgCl_2$. This activation time and temperature may vary between laboratories within certain range. For any further advance in cell design, it would be necessary to recalibrate the activation process to determine the optimal conditions.

Thermal annealing and chloride treatment appear to have separate mode of action in the activation process, with some overlap in areas such as recystallisation. This will be explored further in the following chapter.

5.6 Conclusion

The relationship between duration of air annealing with $MgCl_2$ and the device electrical parameters has been explored. The findings were as follows;

- Air annealing with $MgCl_2$ increases device performance. Over-treatment causes a subsequent decline.
- The increases are secondary to J_{SC} and V_{OC} improvements.
- The highest performing devices combine the highest levels of shallow doping across the depletion region with lowest trap energies and cross sections.
- There may also be a change in transport mechanism in the most optimised cells, away from the multi-step tunnelling which is seen in under- and over-treated devices.
- An equivalent circuit of a parallel $R-C$ in series with a parallel $R-CPE$, with a series resistance is able to describe the equivalent circuit.
- The series resistance in both AC and DC analysis is at a minimum in the best performing cells.
- The variation of deep trap energy levels with treatment time is thought to indicate modification of the grain boundary potential.

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6. Investigation of the effects of annealing with and without chlorides

6.1 Introduction

In the previous chapter the duration of chloride annealing treatment was found to have a impact on cell working parameters, creating an optimised cell before causing deterioration. Without further investigation it is not possible to attribute changes to the chloride treatment specifically, as annealing alone has been reported to have a beneficial impact on electrical conductivity in polycrystalline CdTe solar devices [1, 2] and single crystal CdTe [3]. In thin polycrystalline films, the increased crystallinity and grain size from annealing are thought to be beneficial. However, neither of these apply to single crystals, which also show improvement from annealing at temperatures of $\sim 400\,^{\circ}\mathrm{C}$. It has been postulated that the improvements are related to a reduction in sub-band gap defects, and removal of structural defects such as stacking faults.

The two studies considered in this chapter compare chloride treated samples with devices which have only been annealed. The impact on performance, current transport, traps and electrical behaviour is investigated and discussed.

6.2 Description of samples examined in this chapter

6.2.1 CdTe cells to identify the effects of window layer type on the outcomes of various annealing protocols (Series 621)

Whereas the experiments in chapter 5 explored a variety of annealing times and temperatures, this compact study simply compared six sample plates prepared in three ways as shown in figure 6.1; as-grown, annealed without chloride application, and annealed following chloride application. The samples had either CdS or CdS:O as a window layer.

Six sample plates were used in this study. All were grown in-house by Dr. M. Alturkestani. TEC6 soda-lime glass supplied by NSG (coated with SnO_2:F) was used as the substrate. Three sample plates had a 120 nm CdS:O layer grown through RF sputtering in an argon atmosphere with 5% O_2, whilst the other three had the same thickness of CdS grown (i.e. argon atmosphere only). Following this step, all six sample plates had a ~4 µm CdTe layer deposited by CSS. Post-growth treatments were conducted as shown in table 6.1. Cells undergoing chloride treatment were etched for 15 s with NP solution prior to 1 M aqueous $MgCl_2$ application. All cells were then etched for 15 s with NP solution prior to deposition of Au contacts through evaporation. The annealing step for both 'chloride treated' and 'annealed only' devices was undertaken at 400 °C for 20 min. This temperature and time combination was chosen to produce effective devices. However the devices were not optimised for maximum performance. The chloride treated samples were air annealed in a tube furnace, whilst the annealed only samples were heated in air atmosphere in a clean box furnace.

Sample	**Buffer**	**Chloride treated**	**Annealed** 400 °C for 20 min
621/1	CdS	No	No
621/2	CdS	No	Yes
621/3	CdS	Yes	Yes
621/4	CdS:O	No	No
621/5	CdS:O	No	Yes
621/6	CdS:O	Yes	Yes

Table 6.1: The post-growth preparation of cells in study 621.

6.2.2 CdTe cells to compare the effects of no treatment, heat treatment alone and heat treatment with $MgCl_2$ (Series 622)

For this study thirty-two sample plates were grown in-house by Dr. M. Alturkestani. TEC6 glass was used as the substrate for growth of a 120 nm CdS layer by RF sputtering in an argon atmosphere. A ~4 µm CdTe layer was deposited by CSS. All sample plates bar one (the as-grown sample) underwent post-growth processing, which involved a 'first stage annealing' process for all samples. This was performed in a box furnace under air atmosphere, and was varied in temperature and duration as shown in table 6.2 (400 - 550 °C for 0 - 120 minutes). Following this step, selected cells underwent the usual $MgCl_2$ processing (application of $MgCl_2$ followed by air annealing, the 'second stage annealing'). The sample plates were matched pairwise such that each chloride treated cell with a particular time/temperature first stage annealing combination had a similar 'control' sample plate which had not had the second stage anneal.

The 'second stage' chloride treatment and anneal proceeded as follows: first the cells were etched using NP solution for 15 s before rinsing with DI water, then sprayed with aqueous 1 M $MgCl_2$. They were then air annealed in a tube furnace for 35 minutes at 410 °C. A second 15 s NP etch was performed for all cells before application of evaporated gold contacts. The chloride treated cells were therefore etched twice, whereas the others only etched once.

Sample	**First stage annealing (no chloride)**		**Second stage annealing (with $MgCl_2$)**	
	T (°C)	***t*** (min)	***T*** (°C)	***t*** (min)
622/1	400	30	410	35
622/2	400	30	-	-
622/3	400	60	410	35
622/4	400	60	-	-
622/5	400	90	410	35
622/6	400	90	-	-
622/7	400	120	410	35
622/8	400	120	-	-
622/9	450	30	410	35
622/10	450	30	-	-
622/11	450	60	410	35
622/12	450	60	-	-
622/13	450	90	410	35
622/14	450	90	-	-
622/15	450	120	410	35
622/16	450	120	-	-
622/17	500	30	410	35
622/18	500	30	-	-
622/19	500	60	410	35
622/20	500	60	-	-
622/21	500	90	410	35
622/22	500	90	-	-
622/23	500	120	410	35
622/24	500	120	-	-
622/25	550	30	410	35
622/26	550	30	-	-
622/27	550	60	410	35
622/28	550	60	-	-
622/29	550	90	410	35
622/30	550	90	-	-
622/31	550	120	410	35
622/32	550	120	-	-
622/33	-	-	410	35
622/34	-	-	-	-

Table 6.2: Post-growth treatment for sample plates in Series 622 including a variety of temperatures, T and times, t for the first stage anneal.

6.3 Results

6.3.1 CdTe cells to identify the effects of window layer type on the outcomes of various annealing protocols (Series 621)

6.3.1.1 Performance

a) Efficiency and working parameters

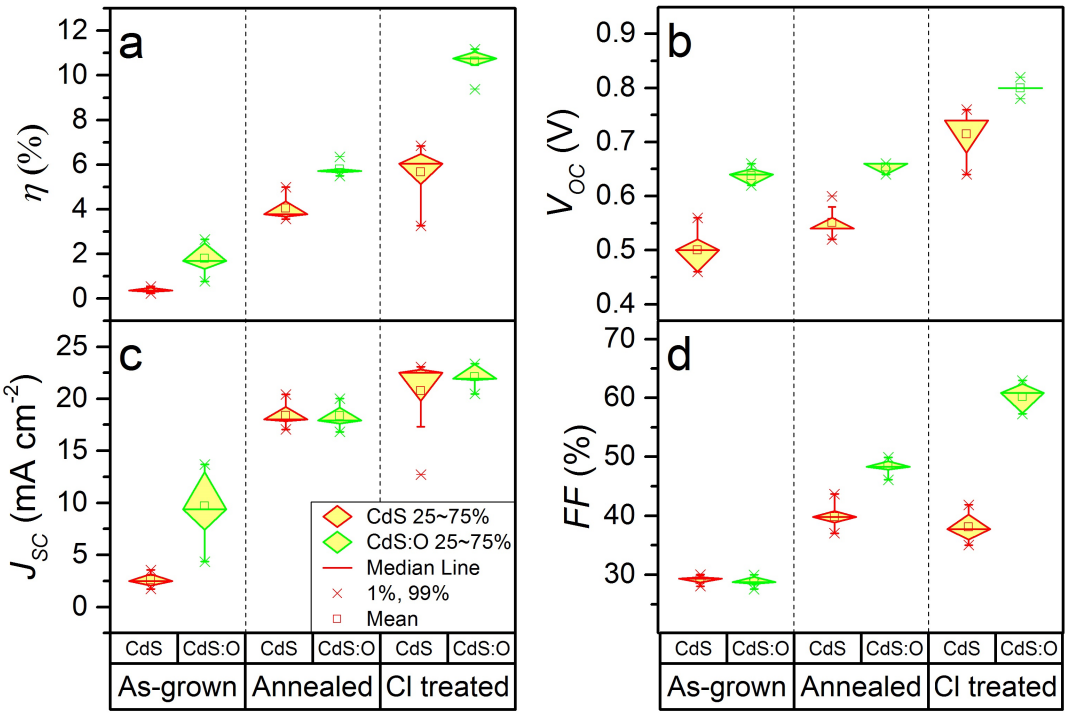

Figure 6.1: Box plots demonstrating the spread of performance parameters for N contact dots per sample plate, (Max $N = 9$) for Series 621: a) efficiency, b) open-circuit voltage, c) short-circuit current density and d) fill factor.

The box plots shown in figure 6.1 show the distribution of the performance parameters for Series 621. It can be seen in panel a) that the as-grown CdS:O sample had a higher efficiency at ~2% than the as-grown CdS device with < 1%. This arises from a markedly higher V_{OC} (~0.65 V for CdS:O, ~0.45 - 0.55 V for CdS) and J_{SC} (5 - 14 mA cm^{-2} for CdS:O, ~2.5 mA cm^{-2} for CdS). Both annealed and chloride treated samples had higher efficiency than the as-grown samples, with the chloride treatment increasing the J_{SC} and V_{OC} more than annealing alone. The best performing sample plate of the series was the chloride treated CdS:O device.

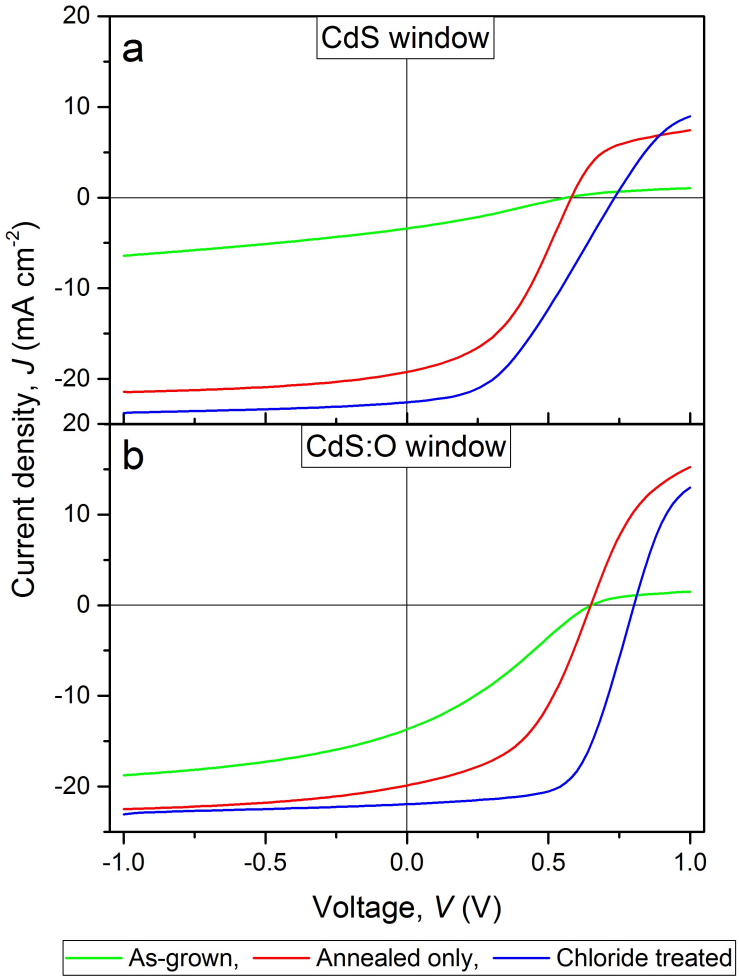

Figure 6.2: Typical $J-V$ curves for Series 621 devices with window layers of a) CdS, and b) CdS:O.

For the six sample plates typical $J-V$ curves are shown in figure 6.2. As expected the chloride treated samples showed the best diode behaviour, with the steeper slope of the CdS:O samples in forward bias showing evidence of a lower R_S than the CdS counterparts. All cells displayed significant roll-over beyond 0.6 V. The turn-on voltage for CdS samples was similar in both annealed and chloride treated cells, whereas for the cells with a CdS:O window layer, the chloride appeared to increase the turn-on voltage to > 0.5 V.

b) EQE

External quantum efficiency data for Series 621 is shown in figure 6.3. At first glance it is clear to see the quantum efficiency of the CdS:O as-grown sample was significantly greater across the wavelength range than its CdS equivalent, and indeed the latter sample showed evidence of a buried junction. For both window layers EQE improved with both annealing and chloride treatments, but there was

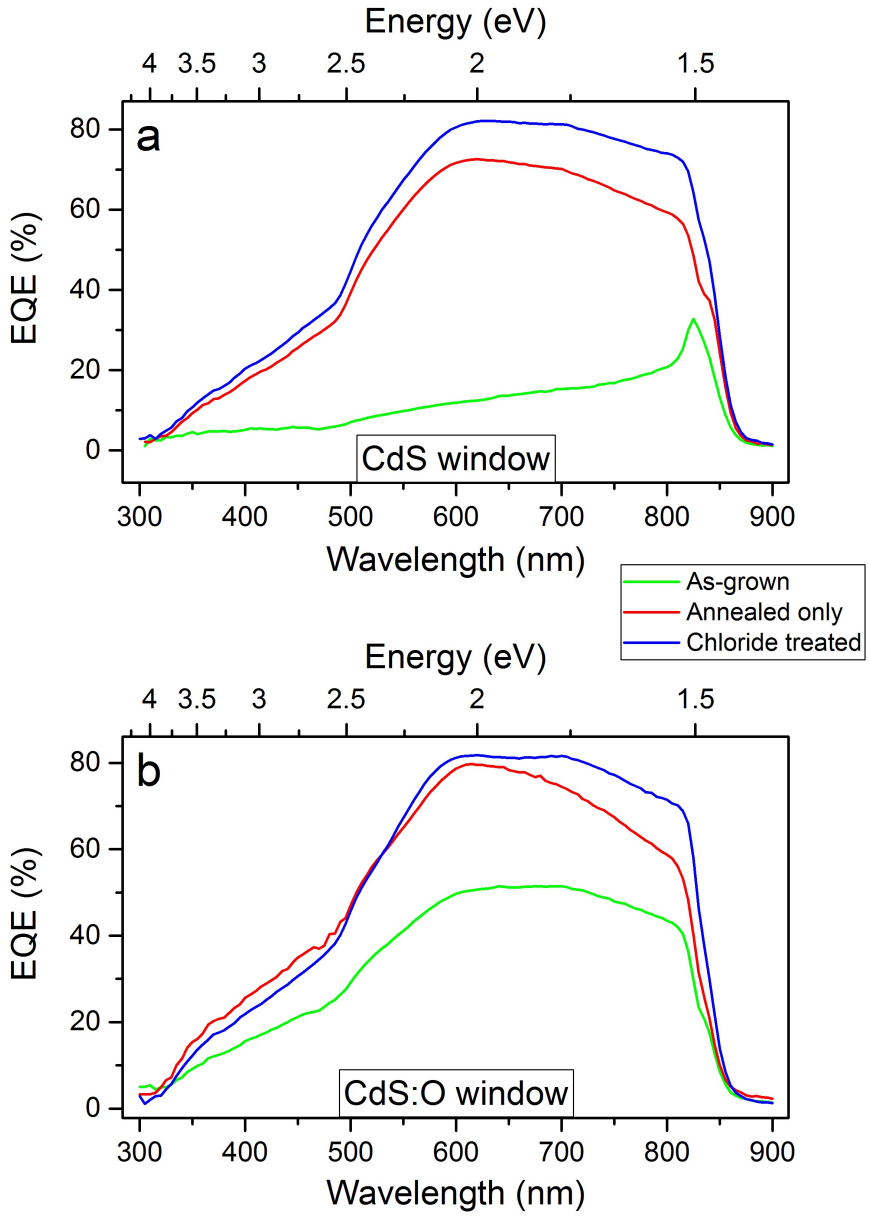

Figure 6.3: External quantum efficiency curves for Series 622 devices with windows layers of a) CdS, and b) CdS:O.

an increase in EQE in the range (600 - 850 nm) when chloride was used. The CdS bandgap was visible in a) and b) at ~2.5 eV, with minimal differences between chloride treated and annealed samples. The CdS:O window appeared to give a slightly higher efficiency in the shorter wavelength region (350 - 500 nm) but the difference was small.

For the sample with CdS:O the EQE step at ~500 nm was more marked than for the similar sample described in section 5.3.2.1, despite both being grown, if not annealed, under similar conditions. Perhaps this was due to the CdS:O segregating to form a CdS/CdS:O bilayer upon annealing, as has been reported elsewhere. Certainly the EQE curves above for both the CdS:O and CdS samples

are similar, despite the CdS:O sample having higher performance. It is therefore speculated that the increased performance of CdS:O was not due to optical effects, but instead to electrical factors. Indeed its fill factor (~60%) significantly outperformed that of the CdS device (~40%).

6.3.1.2 Current transport

a) Main junction

$J-V-T$ studies in dark conditions and under varied illumination were used to determine the dominant transport mechanisms. The dark data is discussed first.

The results from analysing the dark $J-V-T$ data using the multi-step tunnelling model (equation 2.12) are shown in figure 6.4. In panels a) and b) the

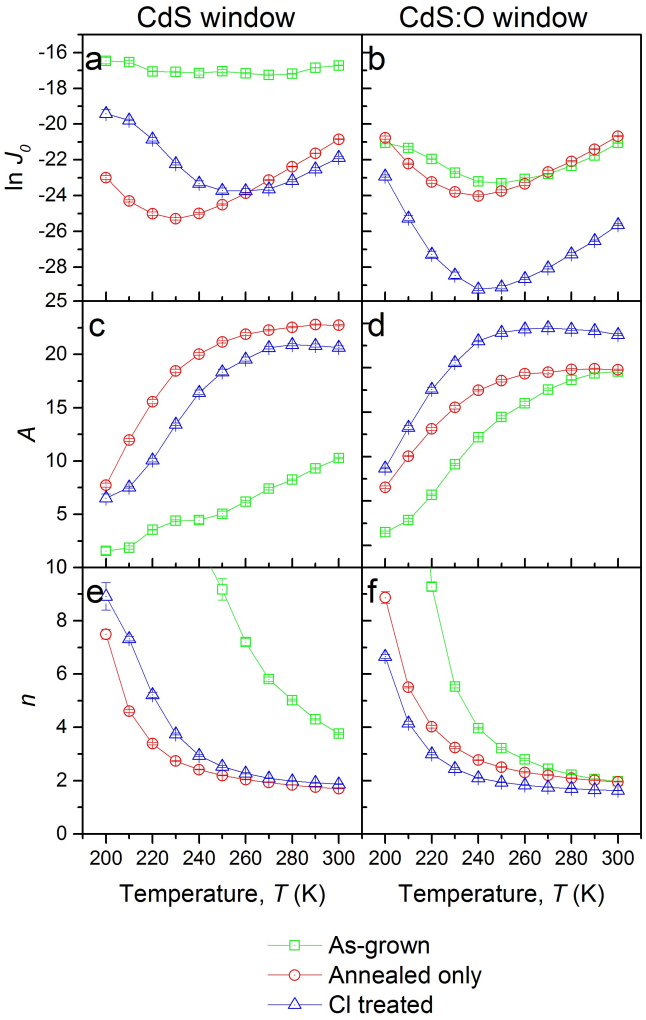

Figure 6.4: Data from $J-V-T$ studies in dark conditions on Series 621 with CdS window samples on the left hand side (a, c, e) and CdS:O samples on the right hand side (b, d, f). The temperature dependent behaviour of a and b) $ln\, J_0$, c and d) A and e and f) n is shown.

behaviour of lnJ_0 can be seen. For temperatures above 250 K all samples had a reduction in reverse saturation current with reducing temperature as is expected (above 270 K for the as-grown CdS sample), but below this temperature anomalous behaviour was apparent. As with the samples analysed in chapter 5, when the data was analysed with a single-diode model this unphysical behaviour disappeared, and lnJ_0 reduced with reducing T across the whole temperature range. This indicates that the multi-step tunnelling model fails to describe the cells below 250 K. For the CdS samples, there appeared to be little difference in lnJ_0 behaviour between the annealed and chloride treated samples, with reverse saturation currents for both being $< 1\,\mathrm{nA\,cm^{-2}}$ (lnJ_0 <-20) at room temperature, these being significantly reduced from $55\,\mathrm{nA\,cm^{-2}}$ ($lnJ_0 \approx -17$) in the as-grown sample. By contrast, for the CdS:O devices the annealed sample was similar to the as-grown, both having $J_0 \approx 0.7\,\mathrm{nA\,cm^{-2}}$ ($lnJ_0 \approx -21$) while the chloride treated sample had much lower values of $J_0 \approx 8\,\mathrm{pA\,cm^{-2}}$ ($lnJ_0 \approx -25$).

The behaviour of parameter A (equation 2.12) is shown in figure 6.4 c) and d). For temperatures above 250 K the as-grown samples were temperature dependent, while the annealed and chloride treated cells were not. As the model failed below 250 K (see above) the changing behaviour in this region is not discussed. Values of n (as calculated from equation B.1) decreased with increasing T to values ≈ 2

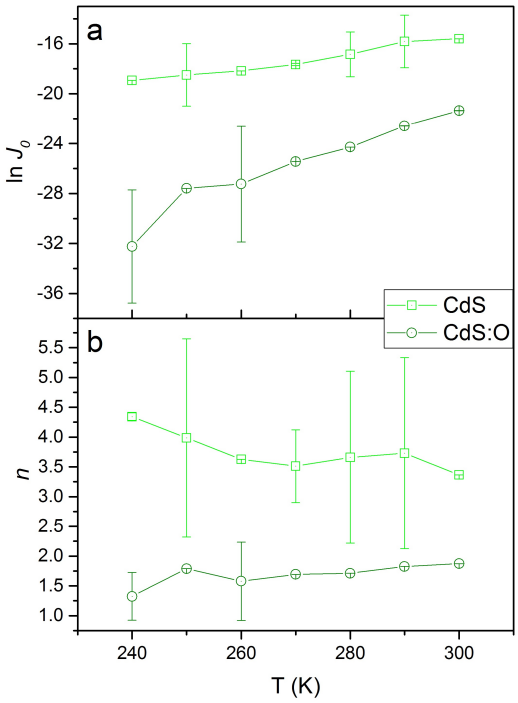

Figure 6.5: Results from analysis of $J-V-T$ in dark conditions on the as-grown samples in Series 621 using the single diode equation to extract a) lnJ_0, and b) n.

Cell	**Window layer**	**Preparation**	N_{nA} (10^{14} cm^{-3})	**Forward bias**		**Reverse bias**			**Back contact**		
				A 300 K	n 300 K	R 300 K	N_t 300 K (cm^{-3})	$\Delta m/\Delta T$ 250-300 K	R_s **calculation**	ϕ_b (eV)	**Fit eq**
621/1	CdS	As-grown	0.3	10.3	3.8	N/A	N/A	N/A	Single diode	0.379 ± 0.024	5.1
621/2	CdS	Annealed only	0.9	22.7	1.7	10,900	1.7×10^{11}	-1.17	Slope	0.4526 ± 0.0018	3.3
621/3	CdS	Cl treated	4.93	20.7	1.9	2,410	7.0×10^{8}	-7×10^{-4}	Slope	0.4304 ± 0.0016	5.1
621/4	CdS:O	As-grown	0.4	19.5	2.0	N/A	N/A	2×10^{-4}	Slope	0.503 ± 0.009	3.3
621/5	CdS:O	Annealed only	0.86	19.7	2.0	15,300	5×10^{7}	-5×10^{-4}	Slope	0.402 ± 0.005	3.3
621/6	CdS:O	Cl treated	2.83	23.7	1.6	3,210	5×10^{7}	-0.01	Slope	0.4436 ± 0.0019	3.3

Table 6.3: The results of analysing $J-V-T$ data for Series 621. The table includes calculated values of slope, A, diode factor, n, and number of tunnelling steps R, which are all calculated from the forward bias data using the multi-step tunnelling model. The reverse bias $J-V-T$ data was used to calculate the trap density, N_t and the exponent m, which can be used to confirm a finding of multi-step tunnelling. N_{nA} was calculated from $C-V$ analysis and will be discussed in the next section. The calculated values for the back contact barrier height, ϕ_b, used either the 'slope' method (section 3.2.3) or fitting to the 'single diode' equation (3.4) to calculate R_S, and which equation was use to calculate ϕ_b. In each case the equation chosen produced the best fit as measured through χ^2 and adjusted R^2. Where not stated, calculated errors for all parameters are in the order of 5%.

at 300 K for all cells except the as-grown CdS device.

When analysed in reverse bias all four treated devices (chloride treated and annealed only) were found to have a proportionality of $ln(J_r/V) \propto -(V_d - C)^{-1/2}$ and a negative gradient of $\Delta m/\Delta T$ (see equations 2.17 and 2.18). This confirms that the multi-step tunnelling model is the dominant mechanism for these samples. The two as-grown samples however did not meet these conditions. When analysed using the single diode equation (3.4) different values for lnJ_0 and n were extracted, as can be seen in figure 6.5. The CdS sample still has a value of $n > 2$ which has no physical meaning. Although the as-grown CdS:O had appeared to fit the multi-step model when analysed in forward bias, the model failed in reverse bias. Good fits were found for this sample's data analysed with the single diode model, with values of $n \approx 1.9$ at room temperature. The current transport for these two samples is discussed later in this section, using illuminated $J-V-T$ data.

In table 6.3, the results of analysis using the multi-step tunnelling model can be seen. For all cells demonstrating evidence of multi-step tunnelling, the number of tunnelling steps, R, was calculated. It can be seen to be higher in the 'annealed only' samples ($R > 10,000$ steps) than the 'chloride treated' samples. This would suggest that the action of the chloride was to reduce the number of tunnelling steps. This may occur through increasing the physical or energetic separation between nearby energy levels, such that the tunnelling from one adjacent trap to another is not thermodynamically favourable.

Unlike the samples in chapter 5 there was no evidence of a change to a process other than multi-step tunnelling in the annealed or chloride treated cells, but that is in part to be expected - the samples in this study were not necessarily maximally optimised, as only one annealing time and temperature was used in this small study, so the samples are therefore at an unknown stage in the optimisation process.

b) Back contact

Data from dark $J-V-T$ studies was used to calculate the back contact barrier height, ϕ_b as can be seen in table 6.3. For the as-grown sample with a CdS window layer the series resistance R_S was calculated from fitting the data to the single diode equation in a manner described in section 5.3.1.2. The slope method was used for the other samples (see Appendix B).

The as-grown CdS sample demonstrated a barrier height of ~ 0.38 eV, lower than that of the CdS:O sample which had $\phi_b \approx 0.50$ eV. Although the latter may appear slightly high, this is still in the range reported in literature (p-CdTe-Au values of 0.53 eV [4], 0.60 eV [5]). The four treated sample plates were found to

have values of 0.4 - 0.46 eV, with no discernible effect from chloride treatment. These values were similar to those seen in similar devices analysed in chapter 5.

c) Behaviour under illumination

For Series 621 $J-V-T$ data was taken under varied intensities of illumination, as described in sections 3.2.1 and 4.3.2.2. Analysis of the data allowed calculation of V_{OC}, diode ideality factor n, and built-in voltage V_{bi}.

In figure 6.6 the behaviour of V_{OC} with temperature can be seen. Despite some scatter in the as-grown samples, all samples displayed linear behaviour of V_{OC} with T above ~250 K, with slight deviation below this temperature in the chloride treated CdS sample (panel a). Extrapolation of this linear behaviour to 0 K allows an estimation of V_{bi} for these samples, with the results being shown in table 6.4. These values may be compared to those calculated from dark $C-V$ analysis (see

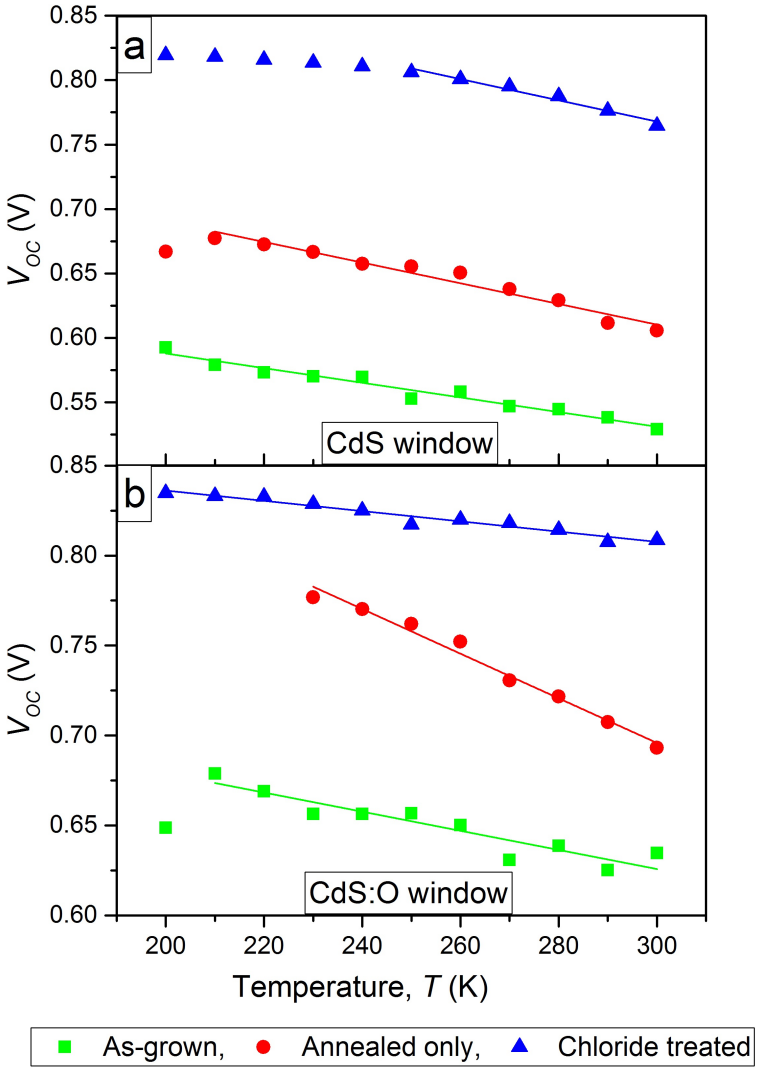

Figure 6.6: Results from $J-V-T$ studies under ~AM1.5 illumination for Series 621 with window layers of a) CdS, and b) CdS:O.

Sample	Window Layer	Preparation	V_{bi} (V)		
			V_{OC} vs T	$C-V$	$n\Delta E$
621/1	CdS	As-grown	0.701 ± 0.009	0.99 ± 0.02	0.34 ± 0.03
621/2	CdS	Annealed	0.85 ± 0.01	0.85 ± 0.02	1.72 ± 0.06
621/3	CdS	Cl treated	1.02 ± 0.02	1.03 ± 0.01	1.48 ± 0.11
621/4	CdS:O	As-grown	0.79 ± 0.02	0.97 ± 0.04	0.73 ± 0.08
621/5	CdS:O	Annealed	1.07 ± 0.02	0.98 ± 0.03	1.88 ± 0.11
621/6	CdS:O	Cl treated	0.90 ± 0.02	0.95 ± 0.01	1.69 ± 0.10

Table 6.4: Comparison of V_{bi} calculations from various methods.

following section). The values found by extrapolation were all consistent with those extracted from dark $C-V$ analysis with the exception of the as-grown samples, where the $C-V$ analysis has over-estimated the value by 0.2-0.3 V. This error in $C-V$ analysis for the as-grown samples is likely to be related to the low frequency at which they were analysed, as had been discussed earlier (see section 5.3.1.3). The final column in table 6.4 is a value of V_{bi} calculated from the product $n\Delta E$ from equation 2.11. For devices where recombination in the depletion region is the dominant form of current transport, n should be equal to 2, $n\Delta E = V_{bi}$, and $lnJ_0 \propto -1/T$ [6]. The as-grown CdS:O sample therefore satisfied all three of these diagnostic criteria, supporting the conclusion that the dominant transport mechanism is recombination in the depletion region.

There is further behaviour that supports this conclusion. For the present samples the value of V_{bi} from light and dark data were consistent with the product $n\Delta E$. On the contrary, for samples having multi-step tunnelling (from $J-V-T$) the V_{bi} and $n\Delta E$ values disagreed. Hence the consistency of the V_{bi} measurements may be used to further confirm the transport mechanism assignment made from using the full diagnostic criteria.

The as-grown CdS sample (621/1) required further investigation to determine the dominant transport mechanism. A further method of determining this uses temperature and illumination dependent V_{OC}, as described in section 4.3.2.2. This can be used to calculate another value of n, where a value of $n = 2/3$, 1 or 2 can indicate Auger, radiative or SRH recombination processes respectively. An example of typical data collected for Series 621 is shown in figure 6.7. The calculated values of n using this process are shown in table 6.5. For the as-grown CdS sample $n = 1.03 \pm 0.13$, which is consistent with ideal behaviour. The values of n for all other samples are included for comparison only, as their transport mechanisms have been identified earlier.

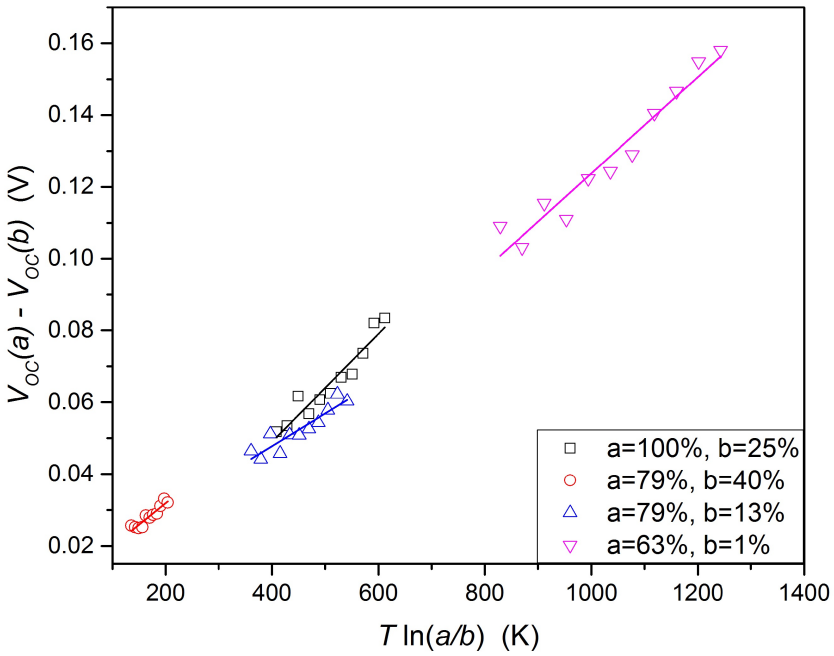

Figure 6.7: A typical example of illuminated $J-V-T$ data used to extract the diode factor, n, from the gradient of the slope using equation 3.2. Parameters a and b are the percentage intensity of AM1.5 spectrum irradiation.

The observed transport mechanisms for Series 621 are now discussed. The finding of radiative recombination in the CdS as-grown sample is consistent with literature reports [7–10]. The presence of oxygen during growth has been thought to be also due to reduced recombination at the CdS/CdTe interface [11], which may explain why the as-grown CdS:O sample demonstrated significantly higher V_{OC} and J_{SC} than the CdS equivalent. As discussed in chapter 5, multi-step tunnelling is a common finding in CdTe cells. Recombination in the depletion region has been reported in literature, including in mechanically etched devices [12].

The effects of illumination on the $C-V$ behaviour of the devices is shown in figure 6.8. These graphs contain data from the chloride treated samples of Series 621 (621/3 and 621/6), and compares the Mott-Schottky and depth density profiles of them. The Mott-Schottky plots displayed considerable changes between light and dark, similar to that seen by Hegedus *et al* [13]. Calculations of V_{bi} from the illuminated CV curves provided similar values to the estimate from V_{OC} vs T however, with values of 0.941 ± 0.008 and 1.09 ± 0.007 for CdS and CdS:O chloride treated samples respectively. Similar changes were present in all of the Series 621 samples, with illumination creating an apparent increase in uncompensated acceptors.

In figure 6.8 a), the dark Mott-Schottky curve is typical for CdTe devices. The

Sample	Preparation	Treatment	n	Transport
621/1	CdS	As-grown	1.03 ± 0.13	Radiative
621/2	CdS	Annealed	1.44 ± 0.18	Multi-step tunnelling
621/3	CdS	Cl treated	3.1 ± 0.8	Multi-step tunnelling
621/4	CdS:O	As-grown	1.8 ± 0.5	Recombination in the depletion region
621/5	CdS:O	Annealed	1.89 ± 0.27	Multi-step tunnelling
621/6	CdS:O	Cl treated	3.0 ± 0.4	Multi-step tunnelling

Table 6.5: The values of n as calculated from $J-V-T$ under varied illumination for Series 621, and the determined dominant transport mechanism from all $J-V-T$ analysis.

illuminated plot is almost straight, and the doping profile in panel b) is almost homogeneous across the sample without the 'U' shape characteristic of dark $C-V$ analysis. For the CdS:O sample in figure 6.8 c) the Mott-Schottky is less curved under illumination than in the dark, but not as linear as the CdS counterpart. This is indicative of an inhomogeneity in the doping profile, which is confirmed in panel d).

6.3.1.3 Shallow and deep levels

a) Shallow levels

$C-V$ analysis under dark conditions was used to determine shallow doping for Series 621. The Mott-Schottky plots from which doping values were extracted are shown in figure 6.9 with the doping density profiles. Similar patterns of behaviour were seen for both CdS and CdS:O window layer devices. The as-grown samples for both window layers were less capacitive than the treated samples, with the chloride treated devices showing the most linear Mott-Schottky plots (panels a and c). The chloride treated samples also demonstrated more homogeneous higher doping across the entire cell (panels b and d). The annealed CdS sample had a very similar profile to the chloride treated device, whereas in the CdS:O sample the chloride appears to have a more marked benefit than thermal annealing alone.

Calculated values of N_{nA}, W_D, and V_{bi} are shown in figure 6.10. In a) an increase in shallow doping from as-grown levels ($< 0.5 \times 10^{14}\,\mathrm{cm}^{-3}$) can be seen for both samples which have been annealed ($\sim 1 \times 10^{14}\,\mathrm{cm}^{-3}$) and chloride treated ($> 1.5\,\mathrm{cm}^{-3}$). The highest value of N_{nA} was seen in the chloride treatment CdS:O sample ($\sim 3 \times 10^{14}\,\mathrm{cm}^{-3}$). The depletion width shown in panel b) was unphysi-

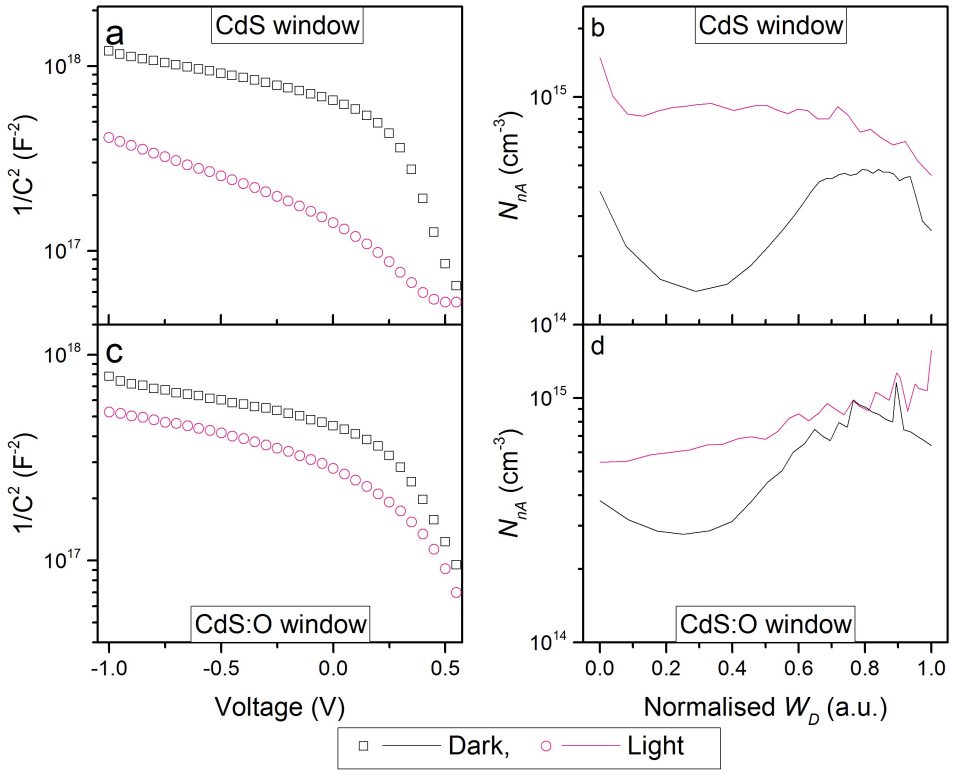

Figure 6.8: Chloride treated samples with CdS (621/3) and CdS:O (621/6) window layers, in darkness and under ~AM1.5 illumination; a) and c) Mott-Schottky plots, and b) and d) depth density profiles.

cally high in the as-grown samples and was comparable to the sample thickness (however, as for the as-grown sample tested in section 5.3.1.3, a low frequency (1000 Hz) was used for the analysis for these poor quality diodes, and there is likely to be a similarly high level of error). The chloride treated samples had similar values of W_D to those seen in devices in chapter 5. Similarly the V_{bi} shown in panel c) had similar magnitude to those seen in chloride treated CdS and CdS:O samples in Series 521 and 522.

The results seem to indicate that chloride treatment has more influence over the doping than thermal annealing, but that both processes help to improve device characteristics. The action of annealing to reduce structural defects may be to release dopants to contribute to cell behaviour, by reducing local compensation. If the primary point of action for the chloride is grain boundary passivation, the two processes working in parallel would be able to produce such observed effects.

b) Deep levels

For Series 621 samples, TAS was undertaken at neutral bias only and the results are shown in figure 6.11. For both as-grown samples, and all the CdS:O samples, two trap signatures were identified, one relatively shallow (<0.15 eV) and one

deep ($\geq 0.2\,\text{eV}$). In the annealed and chloride treated CdS samples only the deep trap was apparent, and had capture cross sections of 10^{-13} - 10^{-14}cm^{-2} and trap densities $> 10^{14}\text{cm}^{-3}$, similar to the treated CdS:O samples. In contrast, the shallow traps seen in both CdS and CdS:O devices had low cross sections of $< 10^{-20}\text{cm}^{-2}$, and fluctuating values of N_t. The shallow trap present in the CdS:O after annealing demonstrated higher trap density than the chloride treated sample, but slightly lower trap energy. For the deep trap there was little difference between the annealed or chloride processed samples.

It is possible the deep traps seen here are measurements of the back contact barrier height, and not an energy level within the band gap. There have been several reports of this in literature, with experimental and theoretical work by Burgelman *et al* demonstrating the presence of a capacitance step in TAS, and transients in DLTS, which could be attributed to back contact effects [14–16]. Such effects have been previously been confirmed experimentally by members of the author's research group [17]. However other groups have also demonstrated that defects visible by TAS were not measuring the back contact [18]. The activation energy values for the deep traps seen in the CdS samples were all consistent with the calculated back contact barrier height ϕ_b (see previous section), whereas

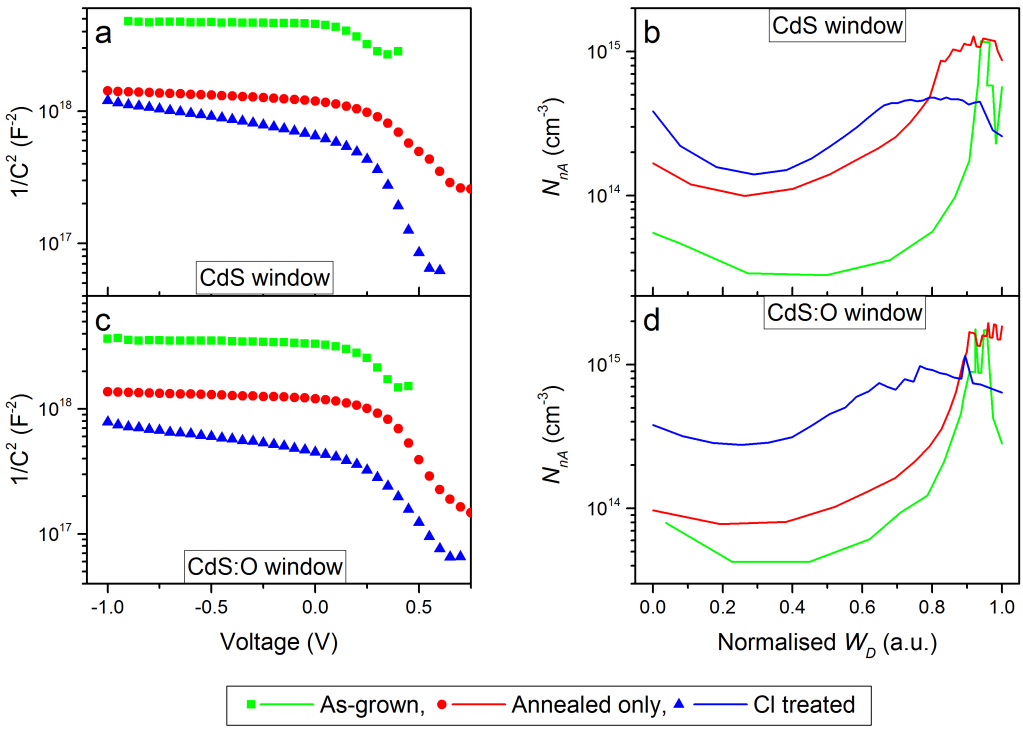

Figure 6.9: A comparison of $C-V$ data for Series 621: CdS window layer samples a) Mott-Schottky plots, and b) doping density profiles, and for CdS:O window layer samples c) Mott-Schottky plots, and d) doping density profiles.

the deep traps in the CdS:O were not. Despite this, both window layers demonstrated similar values of E_{nA}, N_t and σ_{nA} (all of which are similar to values reported in literature), independent of post-growth treatment.

The as-grown CdS sample was found to have similar trap distributions to the as-grown sample in Series 521, with the 20 minute chloride treated sample from that set having a single trap at a ~0.3 eV. The 20 minute chloride treated CdS:O sample studied in Series 522 was found to have two traps with activation energies of ~0.22 eV and ~0.33 eV. Although the number of traps visible was consistent between these chapter 5 devices and their Series 621 equivalents, the trap energies were slightly different. However, as seen in both sample sets in chapter 5, the trap energies changed significantly as a function of treatment time, and it is not known for these Series 621 samples how advanced the optimisation was, so a

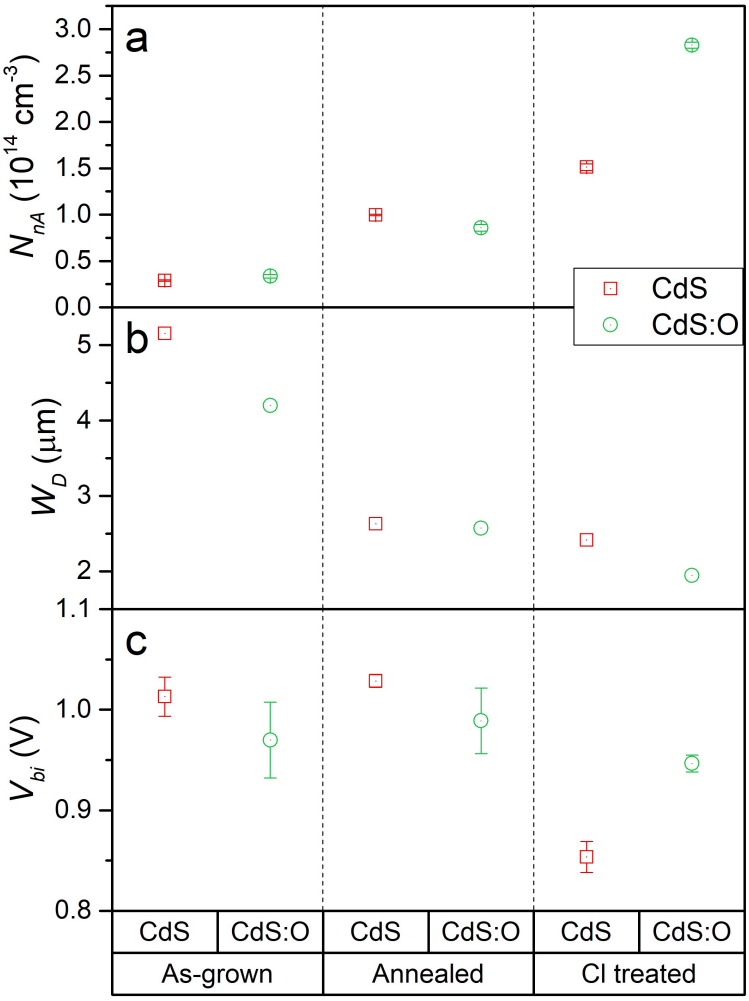

Figure 6.10: Graphs to show values extracted from $C-V$ analysis for sample Series 621; a) uncompensated acceptor density, N_{nA}, b) depletion width, W_D, calculated from $W_D = \varepsilon\varepsilon_0 A/C$ at -1V, and c) built-in voltage, V_{bi}. Both a) and c) are calculated from Mott-Schottky plots (see figure 6.9 and Appendix C).

direct comparison is not expected to show consistent results.

If the energy levels observed in figure 6.11 were interpreted as signatures of particular chemical defects, the complexes responsible are thought to be as follows;

< 0.1 eV The low energy (0.05 eV) levels seen in the as-grown devices and the CdS:O annealed sample are likely to be related to contaminants from the glass. Levels with energies from 0.05 - 0.08 eV have been observed elsewhere and attributed to impurities such as Ag, As, P and Na [19–24]. It may however be the first ionisation state of (V_{Cd}+O_{Te}) (-/0) (0.08 eV) in the CdS:O samples [25].

0.1 - 0.2 eV The 0.19 eV trap visible in the CdS:O as-grown device is thought

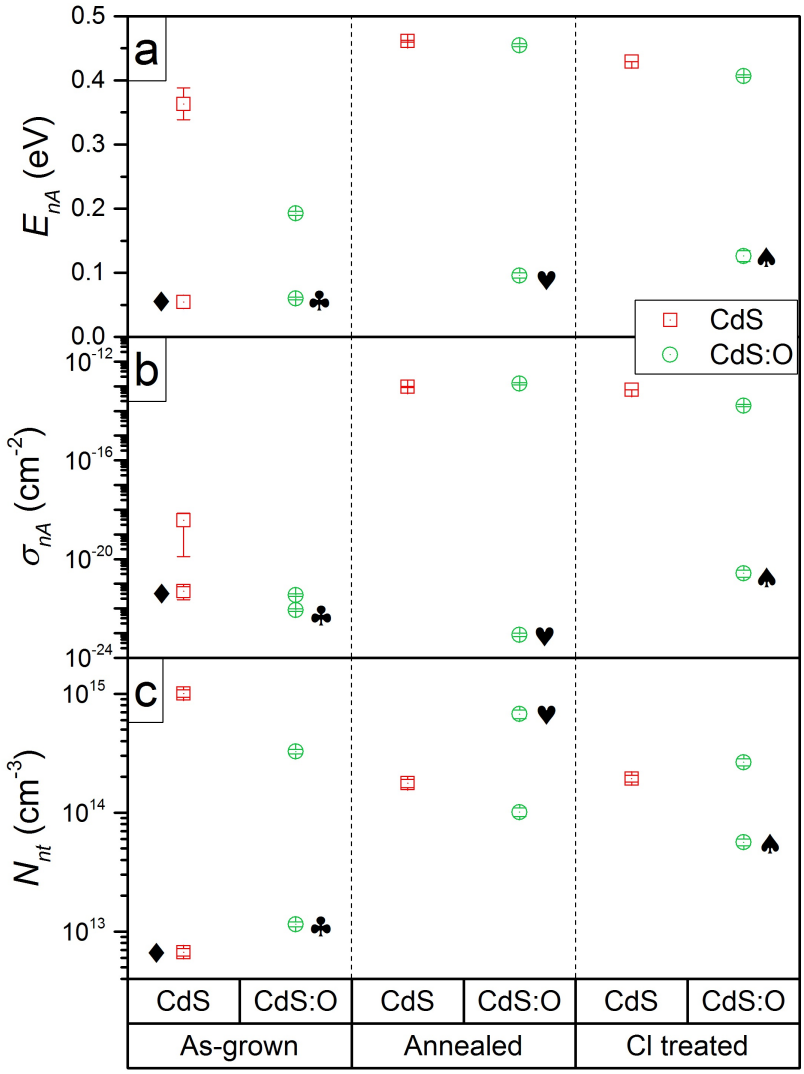

Figure 6.11: Apparent trap parameters of Series 621, as determined through TAS; a) trap energy, E_{nA}, b) cross section, σ_{nA} and c) trap density, N_{nt}. The black symbols are used to correlate trap parameters between vertical groups of panels.

to be related to an oxygen related defect (V_{Cd}+O_{Te}) (-2/-) and has been reported elsewhere, including in non-chloride treated CdTe [14, 19, 25].The shallower 0.12 eV trap observed in the chloride treated CdS:O samples is likely to be the chloride A-centre defect (V_{Cd}+Cl_{Te}) which has an activation energy ~0.13 eV [14, 19, 26].

0.3 - 0.4 eV In the as-grown CdS sample a trap is evident at 0.36 eV. This could be related to a Te_{Cd} defect, or Cu contamination [21, 27–30].

0.4 - 0.5 eV In all the annealed and chloride treated samples, irrespective of window layer, a deep energy level was observed between 0.41 - 0.46 eV. Despite the narrow range, there are likely to be two separate traps being measured. In the chloride treated samples, the substitutional chlorine defect Cl_{Te} has been identified elsewhere with $E_{nA} \approx 0.425$ eV [21, 31]. However, in the samples which were annealed only, the slightly deeper defect could be the interstitial tellurium defect. Te_i, or the (Te_{Cd}+$2V_{Cd}$) complex, both reported in the range 0.45 - 0.48 eV [19, 31–33]

In Series 621, the shallower traps from impurities or the A-centre have only been evident in the as-grown or CdS:O samples. A similar trend was seen in Series 521 and 522, with possible A-centre signatures seen in some CdS:O Series 522 samples, but impurity levels in only the as-grown and 5 minute CdS samples from Series 521. It is speculated the presence of the oxygen in the CdS layer may enable diffusion of, and defect formation from impurity species. In the CdS sample, annealing was sufficient to remove the shallow level, and the (thought to be beneficial to doping) Cu defect [34]. Annealing also removed the oxygen defect from the CdS:O profile, and appeared to promote interstitial or substitutional tellurium-based defects for both window layers. With the addition of chloride treatment, Te vacancies may have been converted to Cl_{Te}. These speculations will be discussed further in chapter 8.

6.3.1.4 Equivalent circuit

AC equivalent circuit methodology as described in section 4.3.4.3 was used to describe the frequency response data for Series 621 at both 0.0 and 0.6 V. Table 6.6 shows the fit quality for the circuits shown in figure 4.3.

As seen for samples in chapter 5, fewer quality fits were possible in forward bias, particularly for the CdS:O samples. Circuit 'c' appeared to be the most appropriate model for both window layer types and voltages. This is similar to the results seen in chapter 5. However, when the R_S from this model were

a

0.0 V		As-grown		Annealed only		Cl treated	
		CdS	CdS:O	CdS	CdS:O	CdS	CdS:O
Equivalent circuit model	a						
	b						
	c						
	d						
	e						
	f						
	g						

b

0.6 V		As-grown		Annealed only		Cl treated	
		CdS	CdS:O	CdS	CdS:O	CdS	CdS:O
Equivalent circuit model	a						
	b						
	c						
	d						
	e						
	f						
	g						

No physical fit
$R^2 > 5$
$5 > R^2 > 1$
$1 > R^2 > 0.5$
$0.5 > R^2 > 0.05$
$0.05 > R^2$

Table 6.6: A schematic to show the range of fit quality for equivalent circuit models a - g (see figure 4.3) to admittance data at a) 0.0 V, and b) 0.6 V for Series 621. The fit quality is indicated by a colour gradient corresponding to R^2, which is the sum of the squares between the data and the fit value. Fits which do not converge, or provide unphysical circuit components are shown in white.

calculated, some unexpected behaviours were noted. These can be seen in figure 6.12. Firstly, the neutral bias resistance was $\sim 50\,\Omega$ in the chloride samples. This is at odds with the data from the previous sample sets. In contrast, the same analysis on chloride treated CdS and CdS:O samples in chapter 5 demonstrated a near zero resistance in optimised samples. Although this could be an indication of a poor equivalent circuit model, a similar R_S pattern was observed with all tested models for this series. Secondly, the AC series resistance varied depending upon the bias voltage. This could be related to the onset of back contact effects,

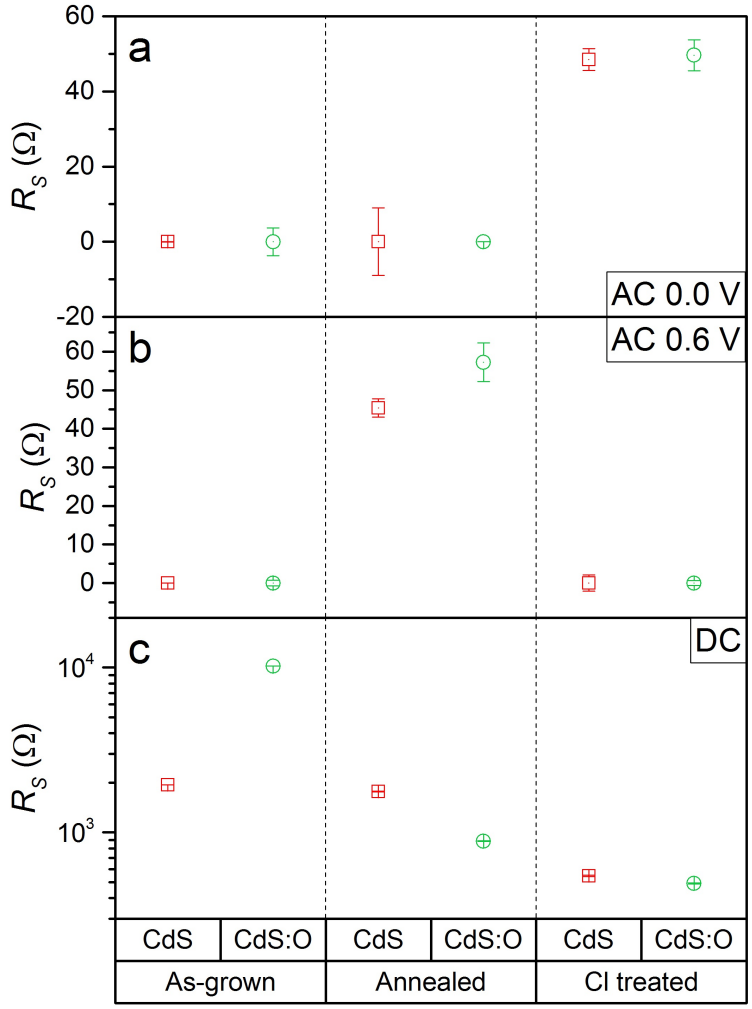

Figure 6.12: The variation of R_S for Series 521 samples, as calculated from a) equivalent circuit 'c' at 0.0 V, b) equivalent circuit 'c' at0.6 V, and c) the DC R_S values calculated by the slope method using $J-V-T$ data at 300 K as comparison.

which occur at lower voltages in the 'annealed only' samples. The behaviour of the DC resistance is shown in figure 6.12 as comparison. The reduced R_S seen in chloride treated samples here agrees with the data from chapter 5, but bears little resemblance to the AC resistances in panels a) and b). While the cause for this unusual behaviour is unknown, it is speculated that a failure to adequately model the equivalent circuit of the devices may be resulting in misleading values of R_S here.

6.3.1.5 Summary of results for Series 621

The findings from analysis of Series 621 are listed below:

- Devices with CdS:O window also had a significantly higher V_{OC}, alongside

an increased turn-on voltage. The J_{SC} and EQE were higher in the as-grown devices, but comparable to the CdS samples after post-growth treatment.

- The samples grown with a CdS:O window layer performed better than those with a CdS layer, even before post-growth processing. The best performing devices were $MgCl_2$ treated cells with a CdS:O window layer.
- Current transport analysis of dark and illuminated devices determined radiative transport as the dominant process in the CdS as-grown device, recombination in the depletion region in the CdS:O as-grown device, and multi-step tunnelling in all processed devices. There were a fifth of the number of tunnelling steps in the chloride treated devices compared to those annealed only.
- Back contact barrier heights did not appear affected by the chloride or annealing processes.
- Although shallow doping levels increased with both annealing and chloride processing, the levels were greater and more homogeneous in the latter.
- The deep trap energy levels changed in processed cells: this is consistent with the continually variable trapping behaviour seen in chapter 5.
- An equivalent circuit model 'c' (figure 4.3) comprising an $R-C$ segment (possibly the main junction), $R-CPE$ component (possibly a distribution of traps and grain boundaries) and a series resistance produced the best fit for all samples.

6.3.2 CdTe cells to compare the effects of no treatment, heat treatment alone and heat treatment with $MgCl_2$ (Series 622)

6.3.2.1 Performance

a) Efficiency and working parameters

The samples studied in this section were CdS/CdTe devices air annealed for a variety of times and temperatures, the 'first stage anneal', following which half of the samples were chloride annealed (in air at 410 °C for 35 minutes, the 'second stage anneal'). The performance data for all 34 sample plates in Series 622 (table 6.2) is shown in figure 6.13. The as-grown sample in this group, sample plate 622/34 (the 0 minute 'annealed only' seen on all panels) can be seen to have an

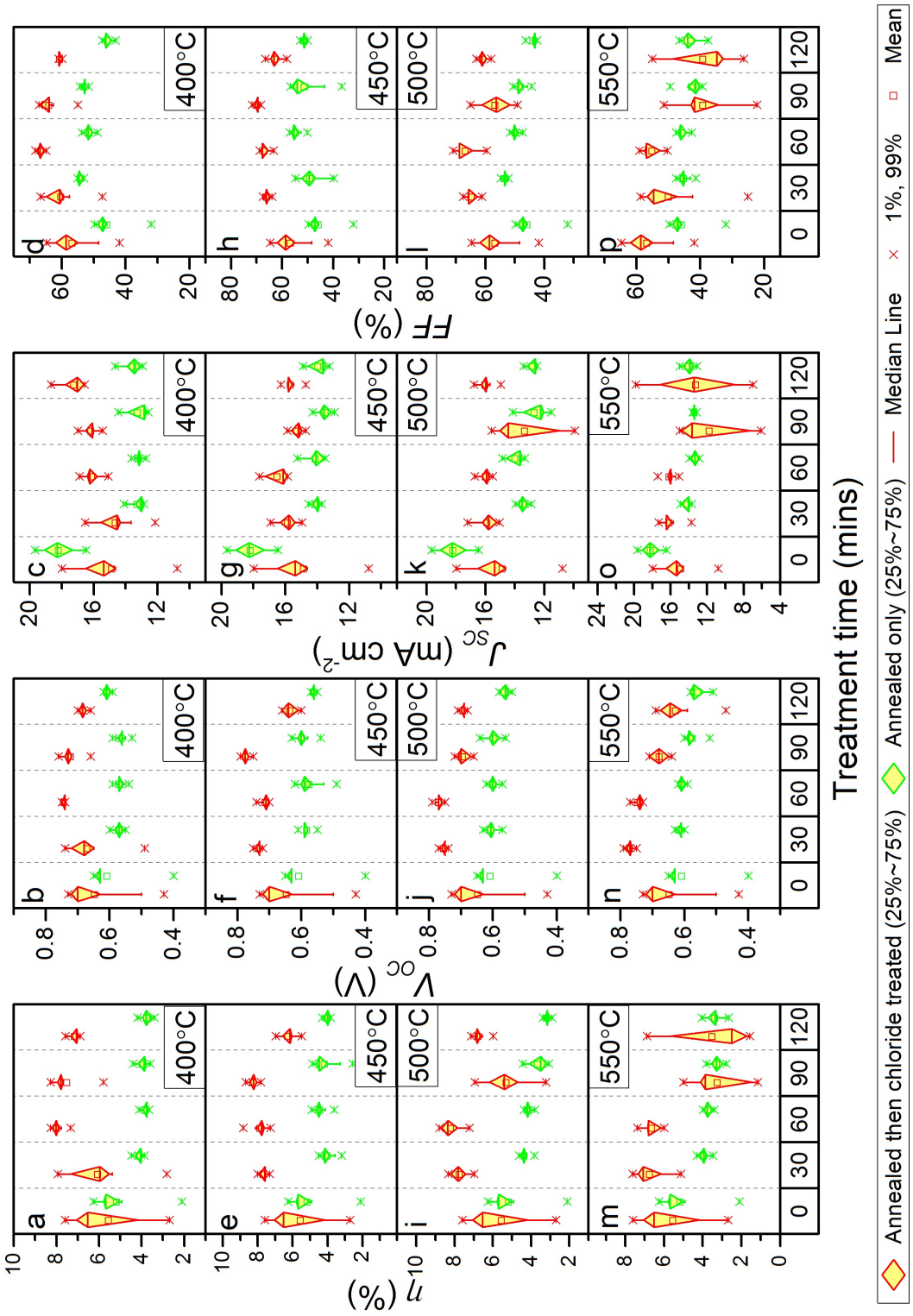

Figure 6.13: Box plots to show performance data for Series 622. Each panel contains data for 10 samples plates air annealed at the stated temperature and time, half of which are then $MgCl_2$ treated; η (panels a, e, i, and m at 400 °C, 450 °C, 500 °C, and 550 °C respectively), V_{OC} (panels b, f, j, and n at 400 - 550 °C), J_{SC} (panels c, g, k, and o at 400 - 550 °C), and FF (panels d, h, l and p at 400 - 550 °C). Each sample plate contained up to 9 contact dots.

unusually high efficiency for an as-grown CdS/CdTe device, with a mean $\eta \approx 5\%$. It also had the highest J_{SC} of the entire series. The sample plate which would represent the usual processing for CdS/CdTe devices is sample plate 622/33, the 0 minute 'annealed then chloride treated' data point seen in all panels. Although the devices on this plate had a higher mean efficiency than the as-grown sample ($\eta \approx 5.8\%$) there was a large range of 3 - 7.5%. This reflects a similarly large range for V_{OC} and J_{SC} in this plate.

In figure 6.13 a), e), i), and m) the efficiency of the samples annealed then chloride treated was higher than those annealed only, with a shallow maximum seen in panel a) at 60 minutes of treatment. This maximum shifted towards shorter anneal durations with increasing temperature. Following the maximum there was a deterioration in η which became more pronounced with higher annealing temperatures. The samples which underwent the first stage anneal only (i.e. not chloride treated) are visible in the same panels, and decreased in efficiency as a function of annealing time. This deterioration was similar for all annealing temperatures.

The V_{OC} results are shown in figure 6.13 b), f), j), and n). Again a shallow maximum was seen in the samples which were annealed then chloride treated. Similar to the efficiency maximum, the peak moved towards shorter anneal durations with increasing temperature, and was followed by a deterioration. The annealed only samples demonstrated a reduction in V_{OC} with anneal duration which was more pronounced at higher temperatures. The J_{SC} in panels c), g), and k) changed little with anneal time in the chloride treated samples but in panel o) (550 °C) there was a deterioration in the average J_{SC} after 90 minutes (a large spread in the J_{SC} of the 90 minute 500 °C appeared to be anomalous). For the samples which were thermally annealed only, the J_{SC} rapidly reduced after 30 minutes of annealing, following which there was invariance of the values. This trend was similar for all anneal temperatures. The fill factor in panels d), h), and i) showed a shallow peak for both chloride treated and annealed only samples, with the chloride treated devices having consistently higher values. The FF in panel p) however (550 °C) decreased with anneal duration in all samples.

The observed increase in efficiency seen in the chloride treated samples appeared to arise largely from an increase in V_{OC}, as can be seen in panels b), f), j) and n). There was little change seen in the J_{SC} (panels c), g), k) and o) until a deterioration was seen at 550 °C after 90 minutes.

On consideration of the performance data, it was decided to investigate the samples treated at 450 °C and 500 °C further as they demonstrated the trends seen in all the samples. The rest of this chapter relates to the investigations performed on 18 sample plates, namely samples 622/9 - 24 and the 0 minute

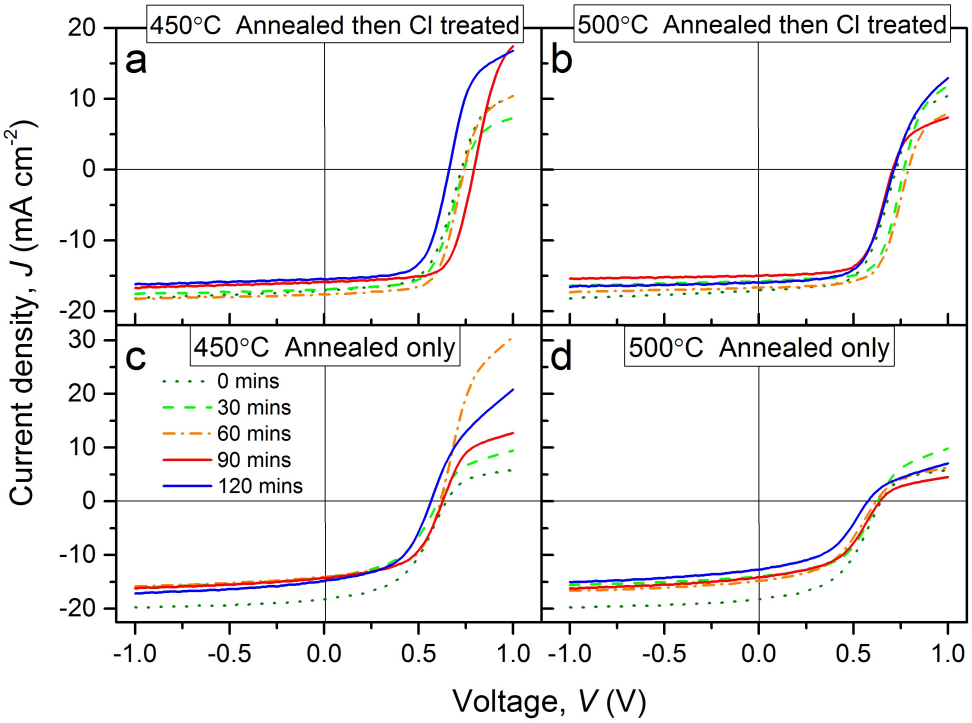

Figure 6.14: $J-V$ curves for the best performing devices on each sample plate for annealing temperatures 450 °C (panels a and c) and 550 °C (panels b and d). Devices processed with chloride after an anneal at the stated time and temperature are shown in the upper panels, while those annealed only are in the lower panels.

samples 622/33 - 34.

Figure 6.14 shows illuminated $J-V$ curves for the best performing devices on these sample plates. There were several key features of the curve that can be seen to change through the addition of the chloride processing. At both temperatures, the reverse bias and low forward bias curve had a constant low gradient in the chloride treated samples (panels a and b), compared to a higher, changing gradient in the annealed samples. A higher J_{SC} was seen in the chloride samples as expected from the performance data. The turn-on voltage was increased to > 0.5 V in the chloride samples, compared to annealed values of < 0.5 V, and there was also an apparent increase in the forward bias slope, indicative of reduced series resistance. The roll-over effect was present in all samples, with the onset occurring at slightly lower voltages in the 'annealed only' samples, particularly in those annealed at 500 °C (panel d). In the chloride treated samples the V_{OC} could be seen to progress with the highest values at 90 mins for the 450 °C and 60 mins for the 500 °C sample. No similar progressive changes are readily apparent in the annealed samples.

The observed $J-V$ changes imply an improved junction in chloride treated samples, with less parasitic resistances and leaking current.

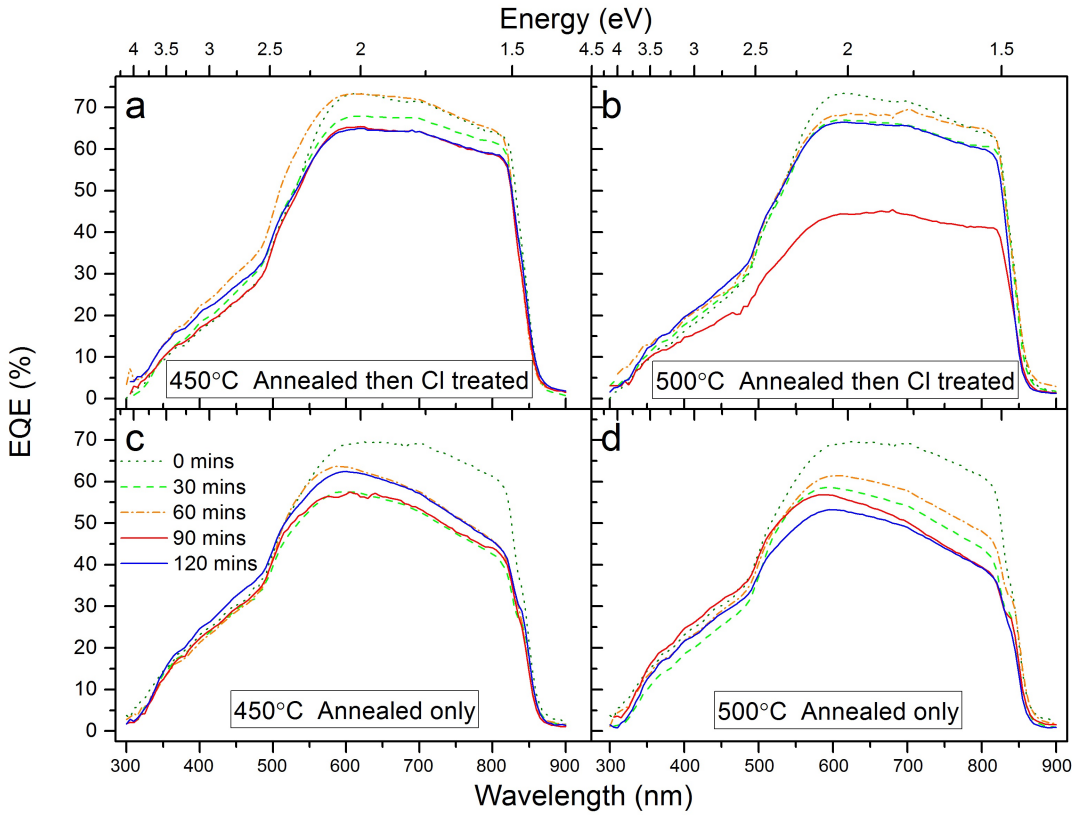

Figure 6.15: Typical external quantum efficiency (EQE) curves of Series 622 devices for annealing temperatures 450 °C (panels a and c) and 550 °C (panels b and d). Devices processed with chloride after an anneal at the stated time and temperature are shown in the upper panels, while those annealed only are in the lower panels.

b) EQE

The EQE data for Series 622 devices annealed at 450 °C and 550 °C is shown in figure 6.15. There are several noteworthy features visible, as listed below.

- The as-grown sample, (0 minute sample in panels c and d) outperformed all of those 'annealed only' in terms of EQE. This was expected from the high J_{SC} seen in this sample's performance data. Those annealed at 450 °C in c) did not significantly change in appearance between 30 - 120 minutes of annealing, whereas the 500 °C anneal (d) seemed to gradually deteriorate with increasing anneal times.

- Aside from the curve amplitude, the only apparent difference between chloride treated and annealed EQE's was an increased signal at longer wavelengths for the former samples. For the chloride treated samples there was little difference between the first stage anneal quantum efficiencies (aside from the 90 minute chloride treated 500 °C device in panel b, which had an anomalously low EQE).

- For the devices processed at 500 °C, the long-wavelength cut-off became subtly sharper with increased annealing times for both chloride treated and annealed samples. This may imply a reduction in Urbach tailing, and therefore a reduction in local disorder in the films processed at the higher temperature [1, 2, 35, 36].

From the above observations, it appears that the chloride treatment in part has acted to improve the EQE in these samples, and that annealing alone has a minimal, or slightly negative, impact on EQE at higher temperatures. This latter point contradicts the EQE seen in samples 621/2 and 621/5, where a significant improvement was observed in annealed only samples compared to as-grown. The unusually high performance of the as-grown sample in this series is likely to be creating a false impression of a negative impact on performance with annealing. However, it does appear likely that high temperature annealing needs to be somewhat shorter than 120 minutes in order to prevent EQE deterioration. This is something that has previously been noted in $CdCl_2$ treated devices [37].

6.3.2.2 Current transport

a) Main junction

$J-V-T$ studies were conducted on Series 622 samples annealed at 450 and 500 °C, and analysed to find values for J_0, A and n as described in Appendix B. The results can be seen in figure 6.16. Examining the lnJ_0 behaviour first, in panels a), b) g) and h), above 260 K there was a linear relationship of lnJ_0 with T. Below this temperature there was a deviation from the linear fit which is most pronounced in the chloride treated samples annealed for shorter times. This was similar to the trends seen in all previous sample sets, where the multi-step tunnelling model failed at lower temperatures. For all Series 622 samples the value of J_0 at room temperature reduced with annealing times of up to 90 minutes. This trend then continued for the samples annealed only at 450 °C, whereas lnJ_0 increases again with longer anneal times for all the other treatments.

The slope parameter A should be reasonably invariant with T in multistep tunnelling, and this seemed to be the case for annealed samples seen in figure 6.16 i) and j) above 260 K. However in the chloride treated samples seen in c) and d) some samples appeared to have a degree of temperature dependence, particularly the sample annealed at 450 °C for 90 minutes. Devices which are dominated by multi-step tunnelling also tend to display a value of n which reduces with increasing T. In panels e), f), k) and l) this was shown to be the case with the exception of this same sample (450 °C 90 minute chloride processed), in which n

had a constant value of 2. It is possible that this sample may have had a different transport process than the others, which all fit the multi-step tunnelling model at this time.

The results from analysis of the reverse bias $J-V-T$ data is shown in table 6.7. The chloride processed sample which was not annealed beforehand did not fit with the multi-step tunnelling model in reverse bias, and the sample had a positive gradient of $\Delta m/\Delta T$. When calculated using equation 2.8 the behaviour of lnJ_0 with T did not fit with the model for recombination in the depletion region either. It also had an unphysical diode ideality factor of $n = 2.4$ at room temperature. The transport behaviour could not therefore be determined for this device. For all other tested devices in Series 622 the $J-V-T$ findings were consistent with multi-step tunnelling. Cells which did not undergo chloride annealing had higher numbers of tunnelling steps than their chloride treated counterparts for first stage annealing times of less than 90 minutes.

The transport mechanism for the Series 622 devices has been shown to be multi-step tunnelling, with the exception of the chloride treated sample which did not undergo a first stage anneal, for which a mechanism could not be determined. This is similar to the trend seen in Series 521, where the transport in the optimised sample could not be established.

b) Back contact

The calculated values for the back contact barrier height ϕ_b are shown in table 6.7. In general the values were slightly lower (0.32 - 0.45 eV) in those samples which had not been chloride treated than those that had (0.37 - 0.47 eV). There was also a minimum in ϕ_b which moved from 90 minutes at 450 °C to 30 minutes at 500 °C (see also figure 6.19 in the following section). The chloride treated samples meanwhile did not appear to change significantly with annealing time.

The decrease in barrier height with air annealing is unexpected and the mechanisms are unclear. However it appears to be the case that chloride treatment returned ϕ_b to a value ~0.40 eV. The chloride treated samples displayed more invariance in ϕ_b despite having two etching steps during manufacture. This is consistent with the finding of Proskuryakov *et al*, who demonstrated that after 10 seconds of etching time, the barrier height does not change with increased etching time [24].

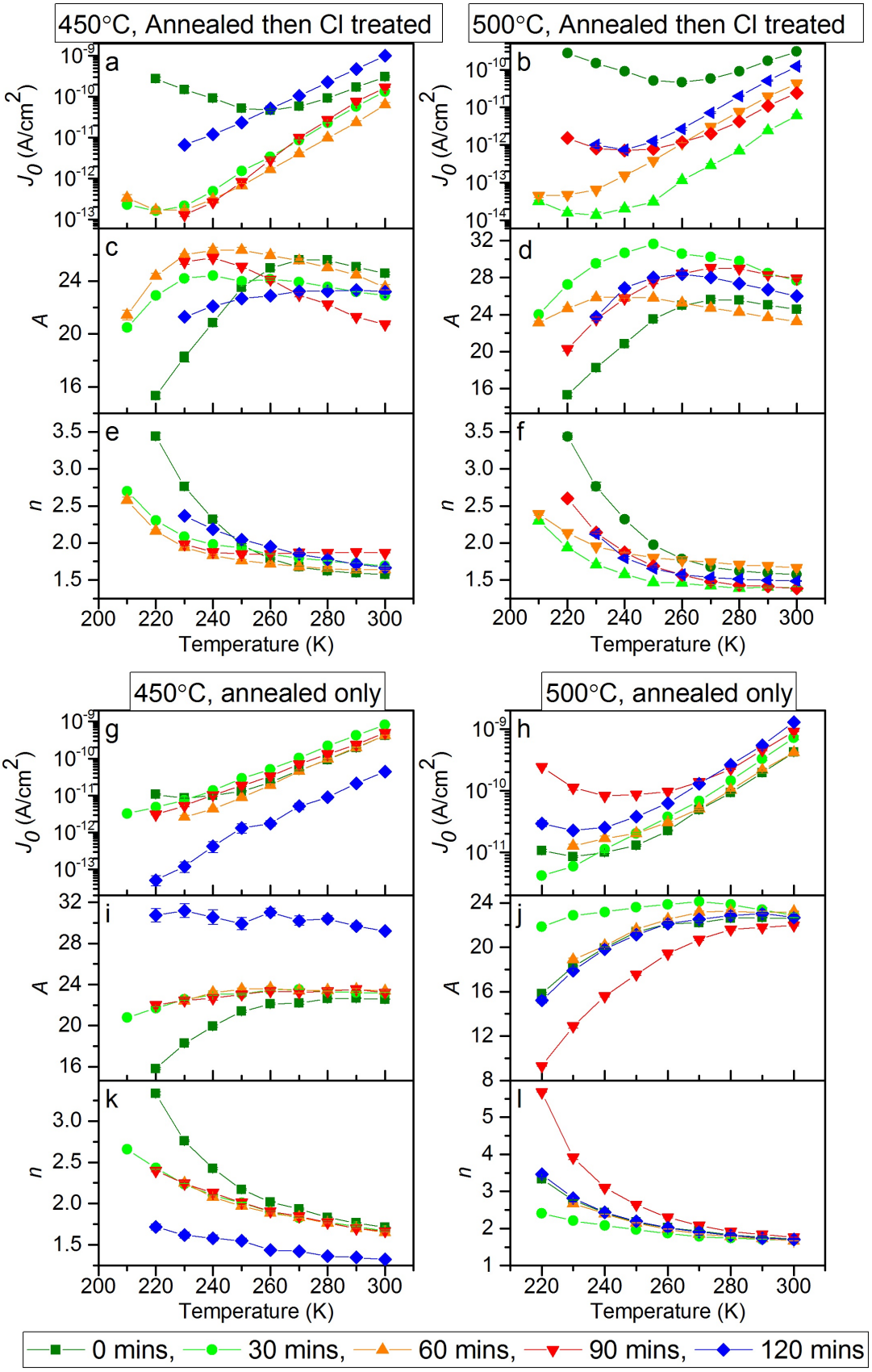

Figure 6.16: Data from $J-V-T$ studies on Series 622 for anneal temperatures 450 °C (left hand side) and 500 °C (right hand side). The upper 6 panels show data for the chloride treated samples, and the lower 6 show annealed data only. Each panel contains information from 5 sample plates, and plot temperature behaviour of $ln\, J_0$ (a, b, g and h), A (c, d, i and j) and n (e, f, k and l).

Sample	**First stage annealing**		**Chloride annealed**	N_{nA}	**Forward bias**		**Reverse bias**			**Back contact**		
					A	n	R	N_t	$\Delta m/\Delta T$	R_s	ϕ_b	**Fit eq**
	T (°C)	t (min)	410 K 35 mins	(10^{14} cm^{-3})	300 K	300 K	300 K	300 K (cm^{-3})	250-300 K	**calc**	(eV)	
622/33	-	-	Yes	2.4	24.6	1.57	N/A	N/A	7×10^{-4}	Slope	0.398 ± 0.002	5.1
622/34	-	-	-	0.4	22.6	1.7	24,000	6.8×10^{8}	-0.7	Slope	0.424 ± 0.001	5.1
622/9	450	30	Yes	4.0	19.3	2.0	3,400	3.5×10^{9}	-0.005	Slope	0.431 ± 0.004	5.1
622/11	450	60	Yes	5.4	23.5	1.6	1,700	2.5×10^{7}	-0.6	Slope	0.404 ± 0.001	5.1
622/13	450	90	Yes	8.5	20.7	1.9	1,400	2.9×10^{5}	-1.4	Slope	0.399 ± 0.003	5.1
622/15	450	120	Yes	4.3	23.2	1.7	2,200	5.8×10^{6}	-0.6	Slope	0.388 ± 0.001	5.1
622/10	450	30	-	5.9	11.9	3.25	6,100	1.2×10^{6}	-0.09	Slope	0.387 ± 0.003	3.3
622/12	450	60	-	4.5	23.4	1.7	2,100	4.1×10^{7}	-0.5	Slope	0.377 ± 0.001	3.3
622/14	450	90	-	5.0	22.6	1.7	2,000	8.3×10^{5}	-0.9	Slope	0.352 ± 0.005	3.3
622/16	450	120	-	4.3	29.2	1.3	1,400	7.5×10^{6}	-0.7	Slope	0.410 ± 0.001	5.1
622/17	500	30	Yes	2.9	27.7	1.4	2,300	1.9×10^{8}	-1.7	Slope	0.415 ± 0.005	3.3
622/19	500	60	Yes	6.0	23.3	1.7	1,570	8.3×10^{7}	-0.5	Slope	0.390 ± 0.012	5.1
622/21	500	90	Yes	1.0	27.9	1.4	6,400	1.1×10^{7}	-0.01	Slope	0.402 ± 0.001	5.1
622/23	500	120	Yes	2.9	26.0	1.5	2,600	4.0×10^{7}	-0.007	Slope	0.483 ± 0.003	3.3
622/18	500	30	-	3.2	22.9	1.7	3,000	3.3×10^{8}	-0.8	Slope	0.322 ± 0.009	3.3
622/20	500	60	-	3.6	23.2	1.7	2,600	3.9×10^{9}	-2.6	Slope	0.370 ± 0.002	3.3
622/22	500	90	-	5.8	22.0	1.8	1,800	2.5×10^{10}	-0.02	Slope	0.375 ± 0.006	3.3
622/24	500	120	-	4.8	22.7	1.7	2,100	1.8×10^{7}	-0.3	Slope	0.414 ± 0.002	3.3

Table 6.7: Results for $J-V-T$ analysis of Series 622 in forward and reverse bias, see section 6.3.2.2 for details

6.3.2.3 Shallow and deep levels

a) Shallow levels

A comparison of the doping density profiles is shown in figure 6.17. The acceptor density in all chloride treated samples annealed at 450 °C (panel a) was increased compared to the usual processing (0 minute sample). Although the highest value of N_{nA} in this plot was comparable to the annealed only samples in panel c), the doping was less 'U' shaped in the chloride treated samples. Those devices annealed at 500 °C in panel b) had a less homogeneous doping profile than their lower temperature counterparts. For the annealed only samples in panels c) and d), after an initial marked improvement from the as-grown, the anneal duration added little further benefit, with the 120 minute sample having a very similar profile to the 30 minute cell.

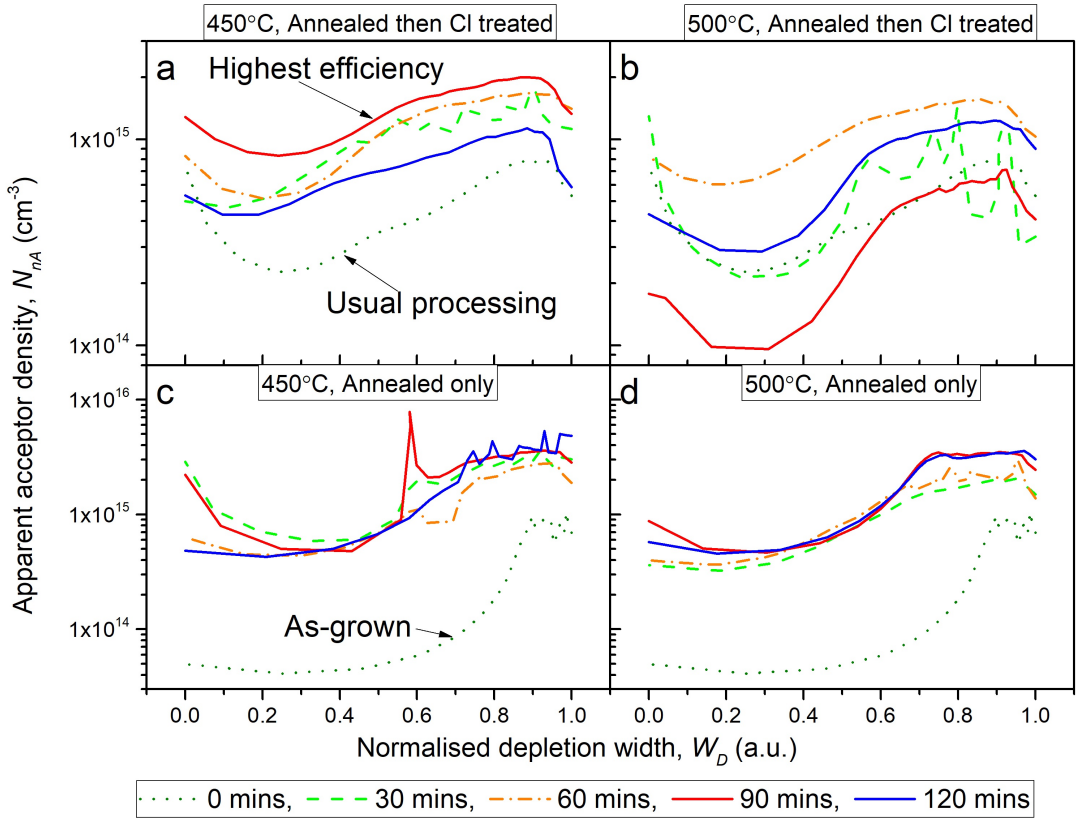

Figure 6.17: A comparison of apparent doping density vs normalised depletion width for samples; a) annealed at 450 °C then Cl treated, b) annealed at 500 °C then Cl treated, c) annealed at 450 °C without chloride processing, and d) annealed at 500 °C without chloride processing.

The values of N_{nA} and V_{bi} as calculated from Mott-Schottky plots are shown in figure 6.18. It can be seen from panel a) that annealing at 450 °C for 30 minutes increased the shallow doping to a higher level than in the device processed in the

usual manner (i.e. chloride treated with no prior anneal). However, for those chloride treated samples which have been annealed before processing, the shallow doping peaked at $8 \times 10^{14}\,\mathrm{cm}^{-3}$ in the 90 minute sample. A similar trend was seen in the samples annealed at 500 °C (panel b), although the bad data point at 90 minutes disturbs the trend. The behaviour of W_D and V_{bi} for both the annealed and chloride treated samples was very similar at both temperatures, with the exception of the bad data point (90 minutes at 500 °C).

The chloride treated samples displayed higher built in voltages despite similar depletion widths to their annealed-only counterparts, with a significant increase evident in the 450 °C samples with a 30-90 minute anneal beforehand. This may be indicative of an improved $p-n$ junction formation in the chloride treated devices. The increased V_{bi} would contribute to the higher V_{OC} in these devices.

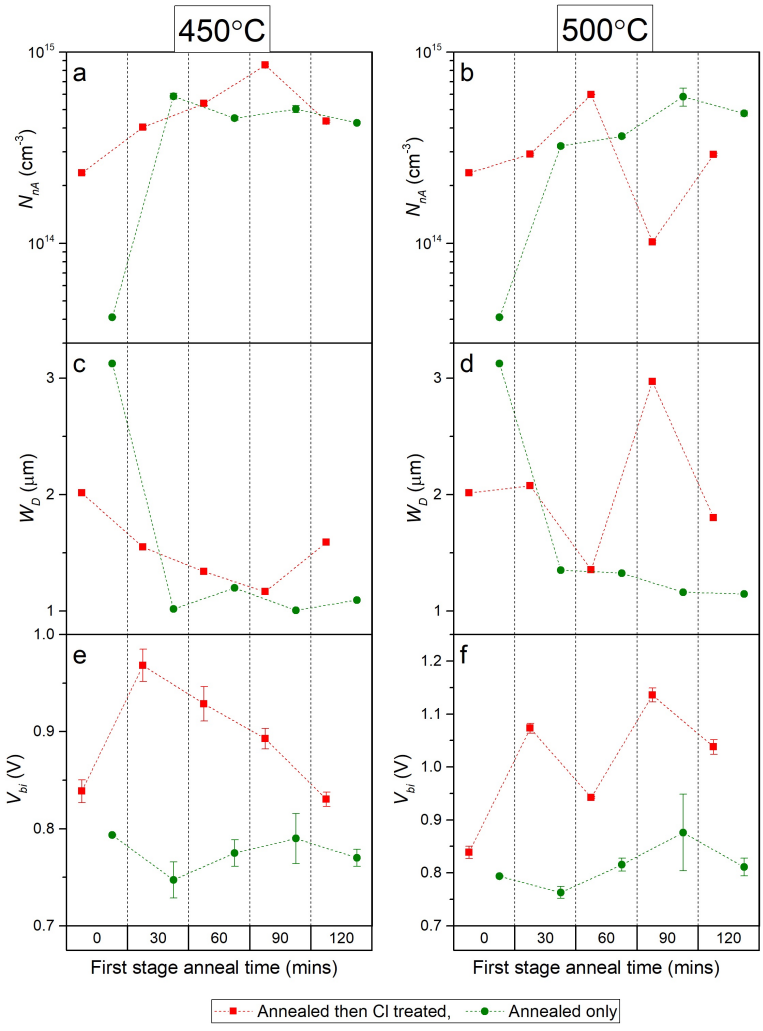

Figure 6.18: Graphs to show values extracted from $C-V$ analysis for sample Series 622; a) uncompensated acceptor density, N_{nA} ($= N_A - N_D$), b) depletion width, W_D, and c) built-in voltage, V_{bi}. Both a) and c) are calculated from Mott-Schottky plots.

b) Deep levels

In Series 622, several devices were found to have three traps by TAS. The ascertained activation energy of one of these traps closely followed the back contact barrier height, ϕ_b. This is demonstrated in figure 6.19. Despite not all of these trap values being consistent with the calculations of ϕ_b extracted from $J-V-T$ data, the similarity in both trends makes it likely that this trap is either a measurement of, or is heavily influenced by, the back contact, as has been reported in $CdCl_2$ treated cells [15, 17]. These traps are not considered in the rest of this section.

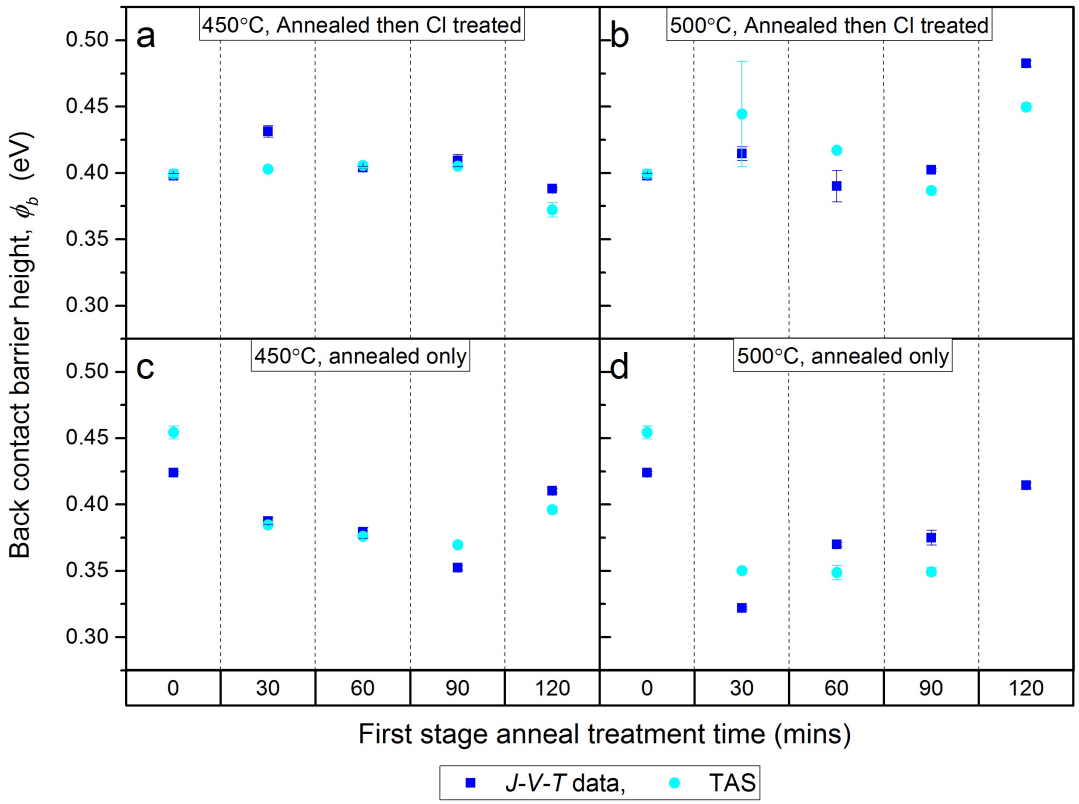

Figure 6.19: A comparison of ϕ_b calculated from $J-V-T$ data for Series 622, and a trap level extracted from TAS data which is likely to be heavily influenced by the back contact; a) Samples annealed at 450 °C for the stated time before chloride treatment, b) Samples annealed at 500 °C then chloride treated, c) samples annealed only at 450 °C, and d) samples annealed only at 500 °C.

The deep level results are displayed in figure 6.20. There was significant variation in all parameters as a function of treatment time. For several devices, both chloride treated and annealed only, there were two traps present. In panels a) and b) the activation energy can be seen to change as a function of annealing time in all cells. The chloride treated cells had generally lower trap energies than their annealed equivalents, with a local minimum in activation energy in

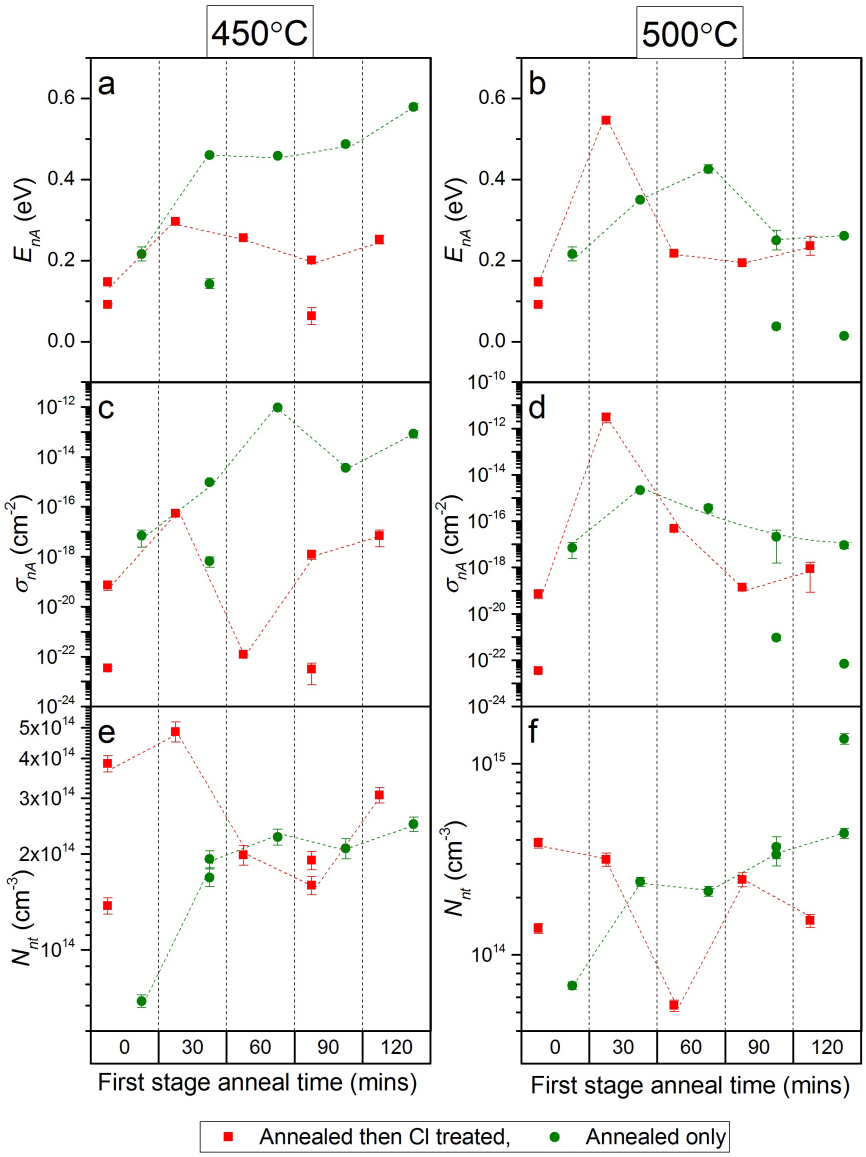

Figure 6.20: Deep trap data for Series 622 calculated using TAS; activation energy for samples annealed at a) 450 °C, and b) 500 °C, capture cross section for cells annealed at c) 450 °C, and d) 500 °C, and trap density for sample annealed at e) 450 °C, and f) 500 °C. The broken lines are used to identify trap parameters across vertical panels.

the best performing cell, the 90 minute device annealed at 450 °C. This sample plate had a corresponding minimum in trap density (panel e), but not in capture cross section. There were similar local minima in E_{nA} and σ_{nA} for those chloride treated samples annealed at 500 °C (panels b and d). In contrast, the annealed only samples at both temperature demonstrated local maxima in E_{nA} and σ_{nA}, with steadily increasing values for N_t.

There are insufficient data points in the 0 - 30 minute anneal range to determine whether the traps visible at thirty minutes are modifications of the traps

seen at 0 minutes, rather than new traps which were either not present at 0 minutes, or not visible to TAS (secondary to having activation energies above the mid gap, for example). However, it seems clear that annealing alone had a negative impact on trap parameters, increasing energy, cross section and trap density. The action of the chloride treatment upon these annealed devices then became more pronounced, with some variations of E_{nA} between chloride treated/annealed only pairs in excess of 0.2 eV. Interestingly, the 30 minute chloride treated sample annealed at 500 °C had significantly higher values for E_{nA} and σ_{nA} that the annealed device, yet had a much higher V_{OC} and twice the efficiency. This indicates that the traps are not the only factor contributing to device performance.

If the calculated trap energies are measurements of discrete trap energy levels, perhaps with modifications by the local lattice, the observed levels in 6.20 a) and b) could have a variety of causes. These are listed below in seven energy ranges in order of increasing magnitude:

0.01 - 0.035 eV This very shallow trap is observed in the samples annealed only at 500 °C for $\geq$ 90 minutes. A theoretical activation energy of 0.02 eV has elsewhere been ascribed to a Na_{Cd} defect [38]. This defect would be feasible in these samples subject to prolonged high temperatures as a contaminant from the glass substrate.

0.06 - 0.09 eV A trap in this energy range was observed in the 0 minute chloride treated sample, and the 90 minute chloride treated after annealing at 450 °C. Levels with energies from 0.05 - 0.08 eV have been observed elsewhere and attributed to impurities such as Ag, As, P and Na [19–24]

0.14 - 0.15 eV This trap was only visible in two samples: the 0 minute chloride treated device and the sample annealed only for 30 minutes at 450 °C. It is likely to be related to the cadmium vacancy defect V_{Cd} (-/0) ($E_{nA} = 0.13$eV) or the slightly shallower A-centre complex (V_{Cd}+Cl_{Te}) [14, 19, 26].

0.21 - 0.29 eV Traps in this range are evident in all samples annealed before chloride treatment, with two exceptions: the 0 minute device, and 30 minute sample annealed at 500 °C. It is also apparent in the as-grown device (0 minutes annealed only) and those annealed only at 500 °C for $\geq$ 90 minutes. In the literature, similar energy traps have been ascribed to the second ionisation state of the V_{Cd} defect, or the copper defect Cu_{Cd}, which has a theoretical activation energy of 0.22 eV [31, 38, 39].

0.35 - 0.36 eV Only appearing in the 500 °C annealed 60 minute sample, this trap is similar in energy to others in literature which have been thought to be related to copper [21, 27, 31, 39, 40].

0.45 - 0.49 eV These traps were only visible in annealed only samples at both 450 °C (30-90 minutes) and 500 °C (60 minutes only). There are many reports of deep levels in this range, variously ascribed to (Te_{Cd}+$2V_{Cd}$), V_{Cd}, or possibly a Te interstitial, Te_i [19, 20, 31–33, 39].

0.55 - 0.59 eV seen in both the chloride treated 500 °C 30 minute sample and the annealed only 450 °C 120 minute sample, this trap is likely to be the Te_i defect, with a theoretical energy of 0.57 eV and has been documented in CdTe previously [21, 22, 38, 41].

It is perhaps significant that the substitutional copper defect Cu_{Cd} (0.21 - 0.29 eV range) is more evident in the chloride treated samples than those only annealed, and is absent in the chloride treated sample which was not annealed beforehand. This may be an indication of the mechanism of improvement in these cells: the anneal improved crystal quality and diffused the copper though the device, whereas the chloride acted to increase the solubility of Cu_{Cd}^{-}, perhaps through introduction of a Cl related donor influencing the Fermi level (and therefore solubility) [31,38,42]. It is speculated that performing the anneal prior to the chloride treatment promotes the formation of Cu_{Cd} defects, which are thought to act as acceptors despite their value of $> 10\,kT$ through partial ionisation [34].

6.3.2.4 Equivalent circuit

The equivalent circuit model fit quality can be seen in table 6.8. The simplest circuit model to provide good quality fits for the chloride treated samples is model 'c', while the annealed only samples can be modelled with both simple models 'c' and 'd' (circuit models shown in figure 4.3).

The series resistances R_S calculated from the circuit model fit are compared in figure 6.21. In panel a) the chloride treated samples are shown, and R_S can be seen to increase to a peak at 90 minutes for both anneal temperatures. On comparing the 450 °C annealed only samples (panel b) with their chloride counterparts, the series resistance appeared lower in the chloride processed devices. However, this trend was lost in the 500 °C annealed samples, which had a low R_S in all devices except the 120 minute sample.

When comparing the component values for each annealed device to its corresponding chloride treated cell, a possible trend was observed for the 450 °C samples as shown in figure 6.22. The process of annealing had the most consistent and pronounced effect on the parallel $R - CPE$ components of model 'c'. The CPE became more capacitive with annealing (CPE^P increased towards 1) while $CPE - T$ decreased (figure 6.22 a), and the resistance $R2$ increased. The

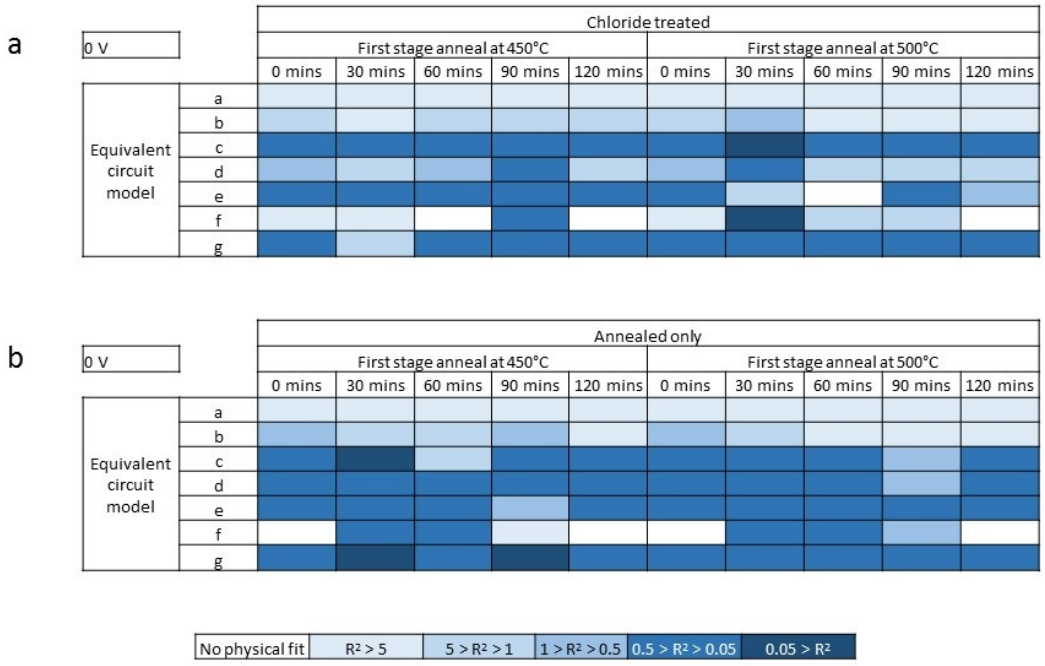

Table 6.8: A schematic to show the quality of fits to equivalent circuit models a - g for Series 622. Details of the circuits are shown in section 4.3.4.3. The fit quality is indicated by a colour guide corresponding to the sum of the squares between the data and the fit. Fits which do not converge, or provide unphysical circuit components are shown in white.

chloride treatment continued the same trend. A similar pattern was observed in some of the 500 °C samples, but not consistently.

6.3.2.5 Summary of results

Analysis of Series 622 has yeilded the results as listed below.

- Air annealing before chloride treatment produced an increase in efficiency and V_{OC}. The peak occurred at shorter anneal durations as the anneal temperature was increased, and was followed by a decline in performance.
- Chloride treatment created a significant increase in V_{OC} over annealed samples, and acted to stabilise the J_{SC}, which decreased with annealing alone.
- All samples demonstrated evidence of multi-step tunnelling (with the exception of the chloride treated sample which was not annealed beforehand). The back contact barrier heights were lower in the 'annealed only' group and changed with annealing duration, but were relatively invariant in the chloride treated cells.

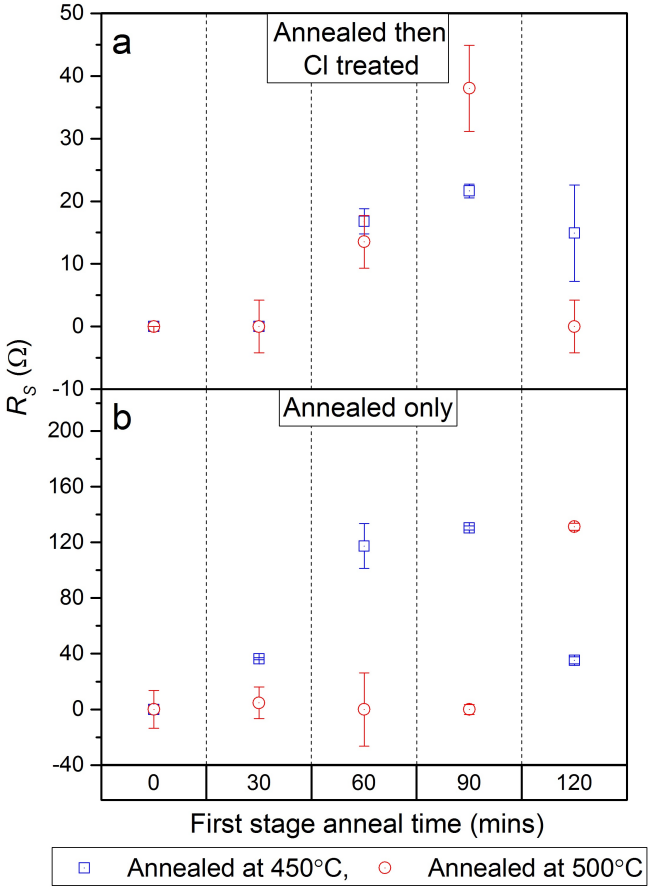

Figure 6.21: Graphs to show the changes in resistor values with anneal duration for Series 622 using model 'c'; a) series resistance R_S for annealed then chloride treated samples, and b) R_S for annealed only samples.

- Shallow doping was highest, and most homogeneously distributed, in the best performing devices. There was a change in doping with anneal duration for the chloride treated devices which was absent in the control samples.

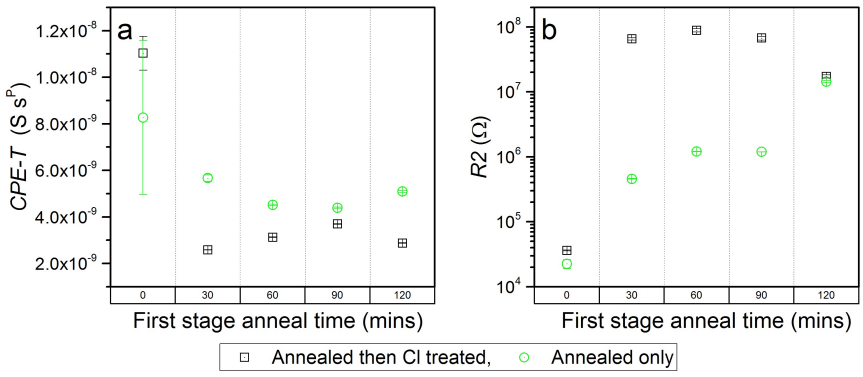

Figure 6.22: Comparison between the chloride treated and annealed only components from model 'c' equivalent circuit analysis; a) the constant phase element CPE_T (The value of CPE_P is $0.9 < CPE_P < 1$), and b) resistor $R2$.

- Deep trap parameters changed with annealing duration, with the best performing (chloride treated) cells having lower activation energy, capture cross section and trap density than the control samples.
- A deep trap which may represent Cu_{Cd} was present in almost all of the chloride treated cells apart from the 0 minute sample (which had no prior annealing).
- Both chloride treated and annealed devices could be modelled by an electrical circuit containing a series resistance, a parallel RC element, and parallel $R-CPE$ element in series. The resistor in the $R-CPE$ appears to change most through the process of chloride treating an annealed sample.

6.4 Discussion

The results from analysis of both Series 621 and 622 are now discussed, with particular reference to the effects of thermal annealing, chloride treatment, or both.

Effect of thermal annealing alone

Thermal annealing without chloride treatment was explored in both Series 621 and 622. In the former, annealing at 410 °C for 20 minutes was shown to increase efficiency and J_{SC} in both CdS and CdS:O samples. This was not the case in Series 622, with an exceptionally high-performing as-grown sample demonstrating larger values of η and J_{SC} than all of the 'annealed only' samples, irrespective of temperature (400 - 550 °C) or duration (30-120 minutes) of the anneal. It is speculated that the anomalous performance of the as-grown device in Series 622 has created a false impression of deteriorating function with annealing, whereas an improvement would be expected, and would be consistent with reported literature [1]. However, annealed samples from both series did demonstrate increased values of N_{nA} from the as-grown samples, and shallower 'U' shaped doping density plots, with higher doping on average across the depletion region. The transport mechanism was found to be multi-step tunnelling for all Series 621 and 622 annealed only samples, consistent with that found for annealing only at 400 °C for 20 minutes [43].

Effect of chloride treatment

Chloride treatment has been shown to be more effective at improving device performance than annealing alone, particularly through increasing V_{OC} in devices

with both CdS and CdS:O window layers, with the latter achieving values of 800 meV. The shallow doping was higher in chloride treated devices than those annealed alone, with the doping density profile describing a shallower gradient in doping across the device, with higher overall acceptor density. Chloride treatment also appears to reduce deep trap energy levels in a manner which annealing does not replicate. Although both annealed and chloride treated cells in Series 621 demonstrated evidence of multi-step tunnelling, the number of tunnelling steps, R, was reduced by almost a fifth in chloride treated cells, implying a reduction in the defect spectrum, either physically or energetically.

Effect of combined treatment (thermal anneal following by chloride treatment)

Devices which were chloride processed after annealing were more efficient than those chloride treated alone, although it was possible to over-anneal the cells with excessive annealing duration and/or temperature. This improvement was largely through a further improvement in V_{OC}, which may be linked to observed increases in V_{bi}. The number of multi-step tunnelling steps, R, did not show a consistent change as a function of anneal duration for the chloride treated devices in Series 621, but did decrease for those annealed only. This could be interpreted as evidence of reducing structural defect density as a consequence of annealing, which the chloride treatment then does little to affect. Shallow doping increased in samples undergoing annealing beyond the level seen in the 0 minute chloride treated or annealed only samples, with the usual 'U' shape doping density curve almost becoming linear in the best performing devices. The improvement in performance for these samples occurred despite an apparent slight increase in trap energy levels from those seen in the cell which had chloride treatment without prior annealing. This may indicate that the performance benefit from annealing prior to chloride treatment arises largely from the improved doping profile, rather than relating to reduced recombination. However, the presence of a possible Cu_{Cd} trap visible in the chloride samples subject to annealing beforehand (and absent in the 0 minute chloride treated sample) is thought to be connected with the increased shallow doping of these samples. It is speculated that the action of the annealing prior to chloride treatment enabled the formation of the dopant Cu_{Cd} defect.

In conclusion, after consideration of the above results, it is speculated that the actions of annealing alone are to reduce crystal defects and improve shallow doping, possibly though promoting diffusion of Cu introduced as a contaminant. This acts to increase current and therefore efficiency.

The presence of copper in these devices is speculated, but the source of the

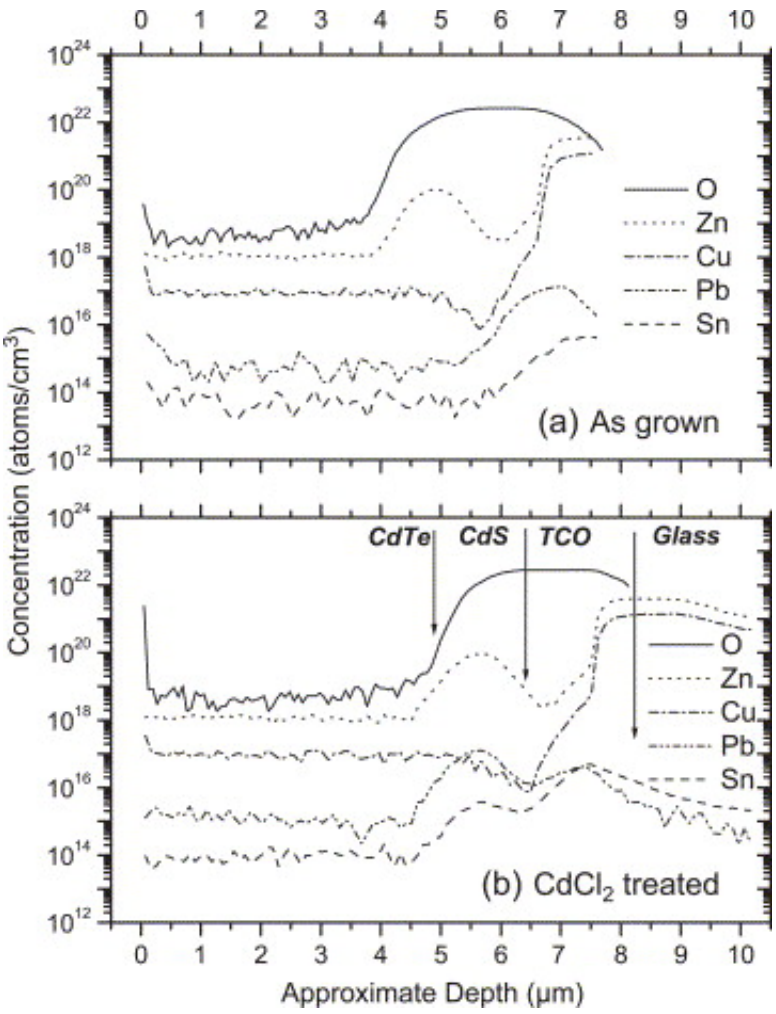

Figure 6.23: Image from 'Effect of $CdCl_2$ activation on the impurity distribution in CdTe/CdS solar cell structures', showing SIMS analysis on CdTe/CdS/FTO/glass devices grown using CdTe of 7N purity [46].

copper contaminant is not clear. Cu contamination determined in CdTe devices reported elsewhere is often attributed to graphite contacts or from $CdCl_2$ processing [5, 44], which are not possible sources here. However, secondary ion mass spectroscopy (SIMS) studies of CdTe devices have previously demonstrated comparatively high concentrations of Cu in non-contacted devices of high purity base materials [45], with higher concentrations still seen in the glass substrate after chloride treatment (see figure 6.23 [46]). Cu is also a very common contaminant in Au [47] and the Au source used for contact formation in these studies has a known trace metal contamination of 15 ppm. It is speculated this may be a source for Cu contamination of the devices studied here.

Treatment with $CdCl_2$ is known to promote recrystallisation in the CdTe more than annealing alone, with grain size dependent on the method of deposition [48, 49]. For these studies, the electrical impact of chloride treatment (i.e.

chloride application then annealing) appear to be two-fold, reducing trap parameters which promote voltage-limiting recombination, and further increasing shallow doping beyond the levels seen on annealing alone. The combination of annealing followed by chloride treatment appears to change the impact of the chloride somewhat, with less effect on reducing recombination, but an increase in shallow doping levels, with a more homogeneous doping profile across the depletion region, and an increase in the observed V_{bi}. This would seem feasible, with the annealing acting to reduce current-limiting defects and diffusing Cu into the CdTe bulk, which then becomes uncompensated through the action of chloride passivation of grain boundaries [50]. The presence of $MgCl_2$ appears to only improve some devices however, those which have been annealed for excessive duration or temperatures do not improve with chloride treatment, despite higher values of N_{nA}, and the resulting devices show a decline in V_{OC}.

6.5 Implications for improving cell performance

Increasing acceptor density in CdTe devices is difficult. In the experiments discussed in this chapter there is limited evidence to suggest thermal annealing prior to $MgCl_2$ activation can improve the acceptor density more than $MgCl_2$ activation alone. For the samples studied here, these devices demonstrated improvements in V_{OC}, FF and efficiency. The use of CdS:O has also been shown to demonstrate improved performance parameters, although as seen from samples in Series 522, inconsistencies in manufacturing of the cells can produce substandard device performance.

6.6 Conclusion

A systematic study has been carried out to discriminate between the effects of simple thermal annealing, annealing with $MgCl_2$, and combined annealing on the performance and deep/shallow behaviours of CdS/CdTe solar cells. It was concluded that:

- As-grown devices display little rectifying behaviour, with low V_{OC}, J_{SC} and efficiency.
- Thermal annealing alone increased J_{SC} and shallow doping.
- $MgCl_2$ treatment increased V_{OC} and R_{SH} while reducing R_S.

- Combined treatment further boosted acceptor density, reduced trap activation energies and improved V_{OC} and FF.
- The likely mechanism of action for the annealing process is through crystal structure modification. For the chloride treatment it is likely to be through grain boundary passivation with Cl and Cu. It is speculated that combined treatment increases uncompensated acceptor states through the creation of more Cu_{Cd} substitutions.

Overall it is feasible that combined treatment improves efficiency but a large sample series would be required to demonstrate this conclusively.

6.7 References

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7. Effects of changing the back contact on cell behaviour

7.1 Introduction

The previous chapters have examined the electrical effects of processing CdTe devices with $MgCl_2$ and annealing, and have noted treatments which act to increase V_{OC}. Additionally it has been reported that use of copper in the back contacts of CdTe can increase V_{OC} and create a more Ohmic contact [1–3]. However over-treatment with Cu, and prolonged stress can cause performance deterioration [4–6], and there is evidence that this is related to diffusion of copper away from the back contact region [7]. Other materials have been considered to provide more stable back contacts, including copper thiocyanate, CuSCN. This material has been used as a hole transporting material in perovskite solar devices and shown to produce open circuit voltages in excess of 850 mV when deposited as a back contact on $CdCl_2$ activated CdS/CdTe cells [8].

This chapter examines two back contact chemistries: in the first, Series 721, Au with varied amounts of Cu was used for the back contact, whereas the second, Series 722, utilised different concentrations of CuSCN instead. Both sample sets were post-growth annealed with $MgCl_2$. The resulting devices were analysed to correlate performance and V_{OC} with the doping density and back contact barrier height.

7.2 Description of samples examined in this chapter

7.2.1 Back contacts with copper

This study comprised four sample plates of identically grown cells post-growth processed with aqueous $MgCl_2$ before application of an evaporated copper layer. The cells were grown in-house by Dr. J. D. Major. TEC7 soda-lime glass supplied by NSG (coated with SnO_2:F) was used as the substrate. RF sputtering in argon was used to deposit a 200 nm CdS layer, followed by a ~4 µm CdTe layer deposited by CSS. Following etching for 15 s in nitric/phosphoric (NP) acid mixture the samples were sprayed with 1 M aqueous $MgCl_2$ and annealed in air in a tube furnace at 410 °C for 25 minutes. A further 15 s etch in NP acid preceded application of evaporated copper layers of depths as detailed in table 7.1, over which evaporated gold contacts were applied.

Sample	**Copper layer thickness** (nm)
721/1	0
721/2	1
721/3	2
721/4	4

Table 7.1: The thickness of evaporated Cu applied to CdS/CdTe solar cell devices (Series 721) prior to Au contact deposition.

7.2.2 Back contacts with copper thiocyanate

Four samples plates were used in this study. All were grown in-house by Dr. L. J. Phillips. TEC10 soda-lime glass supplied by NSG (coated with SnO_2:F) was used as the substrate. RF sputtering in argon was used to deposit a 100 nm ZnO layer and a ~100 nm CdS layer, followed by a ~4 µm CdTe layer deposited by CSS. The sample plates were then etched for 15 s with NP solution prior to spraying with 1 M $MgCl_2$ solution and annealing in air at 400 °C for 28 minutes. The CuSCN layer was deposited by spin coating a CuSCN-containing solution at 400 rpm for 30 s before drying on a hot plate for 10 minutes at 100 °C. The CuSCN was dissolved in either n-propyl sulphide (n-PS) or diethyl sulphide (DES), in concentrations of either 2 or 50 mg ml^{-1}, as detailed in figure 7.2. It was noted

that n-PS appeared a less effective solvent of CuSCN than the DES. Evaporated gold contacts were applied on the CuSCN layer.

Sample	**Solvent**	**Concentration** ($mg\,ml^{-1}$)
722/1	n-PS	2
722/2	n-PS	50
722/3	DES	2
722/4	DES	50

Table 7.2: The solvent (n-propyl sulphide, n-PS, or diethyl sulphide, DES) and concentration (2 or $50\,mg\,ml^{-1}$) used for deposition of CuSCN layers onto CdS/CdTe solar cells by spin coating for Series 722.

7.3 Results and discussion

7.3.1 Back contacts with copper

7.3.1.1 Performance

a) Efficiency and working parameters

The performance of the four sample plates in Series 721 is shown in figure 7.1. The mean device efficiency increased with Cu content with the highest average ($\eta = 10.9\%$) being for 2 nm - although V_{OC} reached a maximum of 0.77 V for 4 nm. In contrast J_{SC} peaked at 1 nm of Cu and deteriorated with increasing Cu content.

Figure 7.2 shows the $J-V$ curves for Series 721. The maximum power point shifts towards higher voltages with increased Cu layer thickness. This appears to be related in part to a reduction in R_S and a significant amelioration of the roll over effect, which appears entirely absent with thicknesses ≥ 2 nm.

The increase in V_{OC} and reduction in J_{SC} with increasing Cu content is consistent with literature reports [1] as is the $J-V$ behaviour [9].

b) EQE

The typical external quantum efficiency plots for Series 721 shown in figure 7.3 vary little with Cu layer thickness, having only slight differences between 500 -

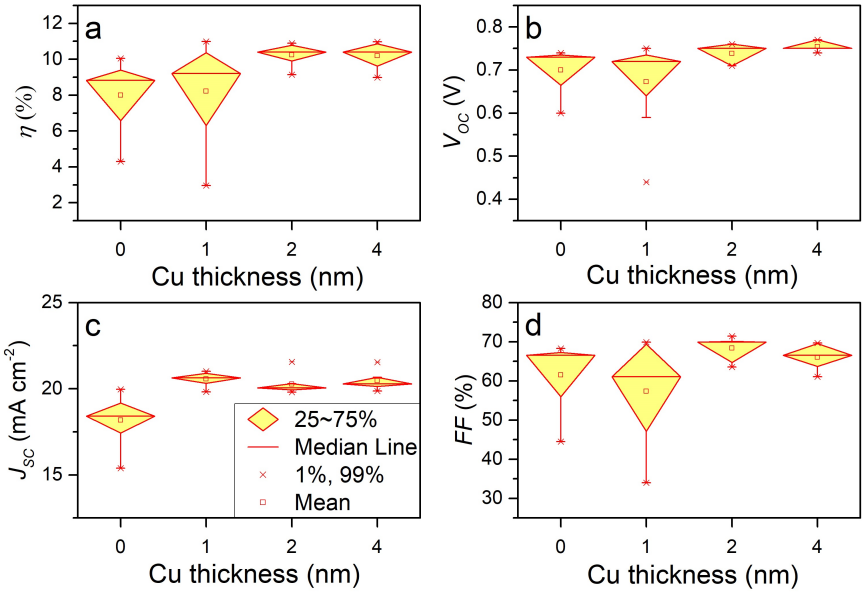

Figure 7.1: Box plots demonstrating the spread of performance parameters for CdS/CdTe cells contacted with Cu (Series 721) for N contact dots per sample plate (Max $N = 9$): a) efficiency, b) open-circuit voltage, c) short-circuit current density and d) fill factor.

850 nm. This suggests the presence of copper has little effect on the optical properties of the devices.

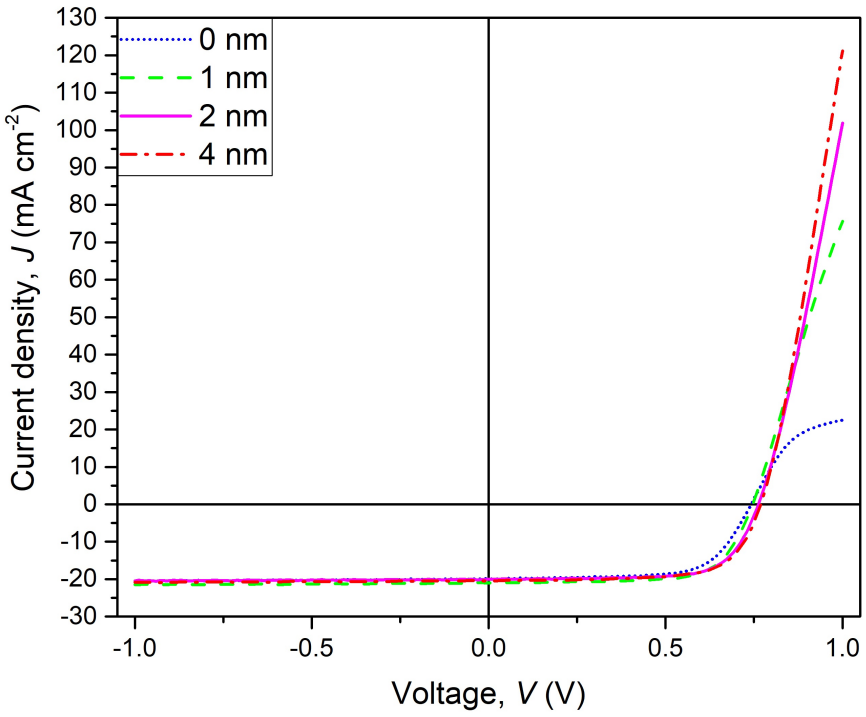

Figure 7.2: Typical $J-V$ curves for CdS/CdTe devices with varying thicknesses of copper in the contacts (Series 721).

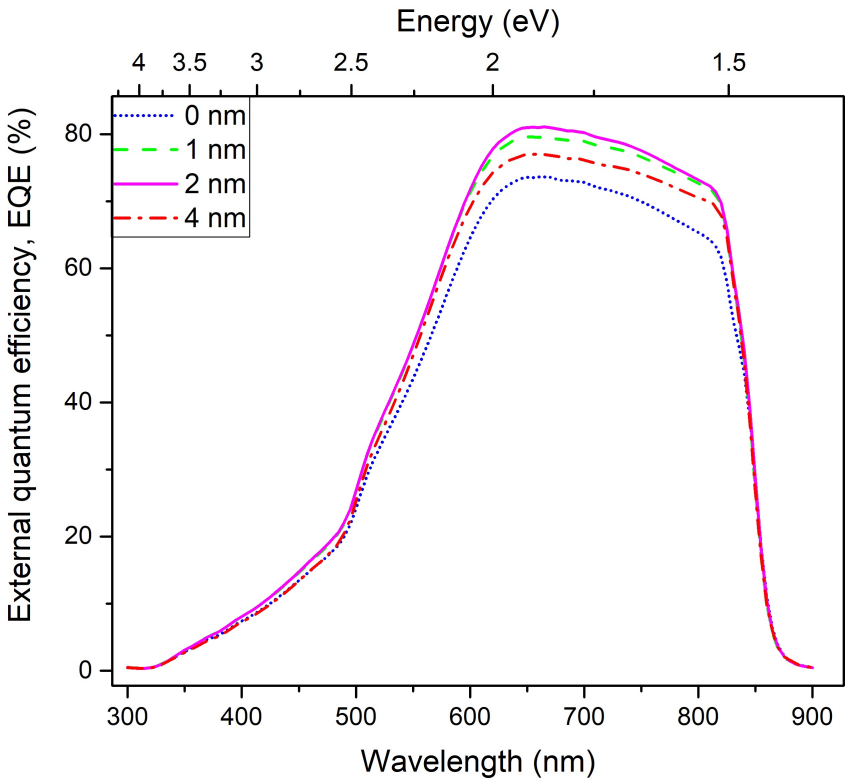

Figure 7.3: External quantum efficiency curves for CdS/CdTe devices with varying thicknesses of copper in the contacts (Series 721).

The best performing sample plate overall had a Cu layer thickness of 2 nm through a combination of high V_{OC} and FF.

7.3.1.2 Current transport

a) Main junction

The transport behaviour for Series 722 was determined through analysis of dark $J-V-T$ data. The behaviour of $ln\, J_0$ with T (figure 7.4 a) is appropriate thermally activated transport for all samples above 250 K, and from 200 - 300 K for the 2 nm sample. In panel b) the slope parameter A is also invariant with temperature over the same ranges, and the value of n decreases with increasing T as is seen in panel c). The 4 nm sample however has an unphysical room temperature value of $n > 2$ when calculated using equation B.1, but has a value of $n = 1.7$ when analysed using the single diode equation (equation 3.4).

The results of analysing the $J-V-T$ data in forward and reverse bias are shown in table 7.3. In reserve bias, all sample plates demonstrated a negative gradient of $\Delta m/\Delta T$, which acts as confirmation of the multi step tunnelling transport mechanism. The number of tunnelling steps, R, can be seen to increase with copper content. Although multi-step tunnelling is common in CdS/CdTe devices,

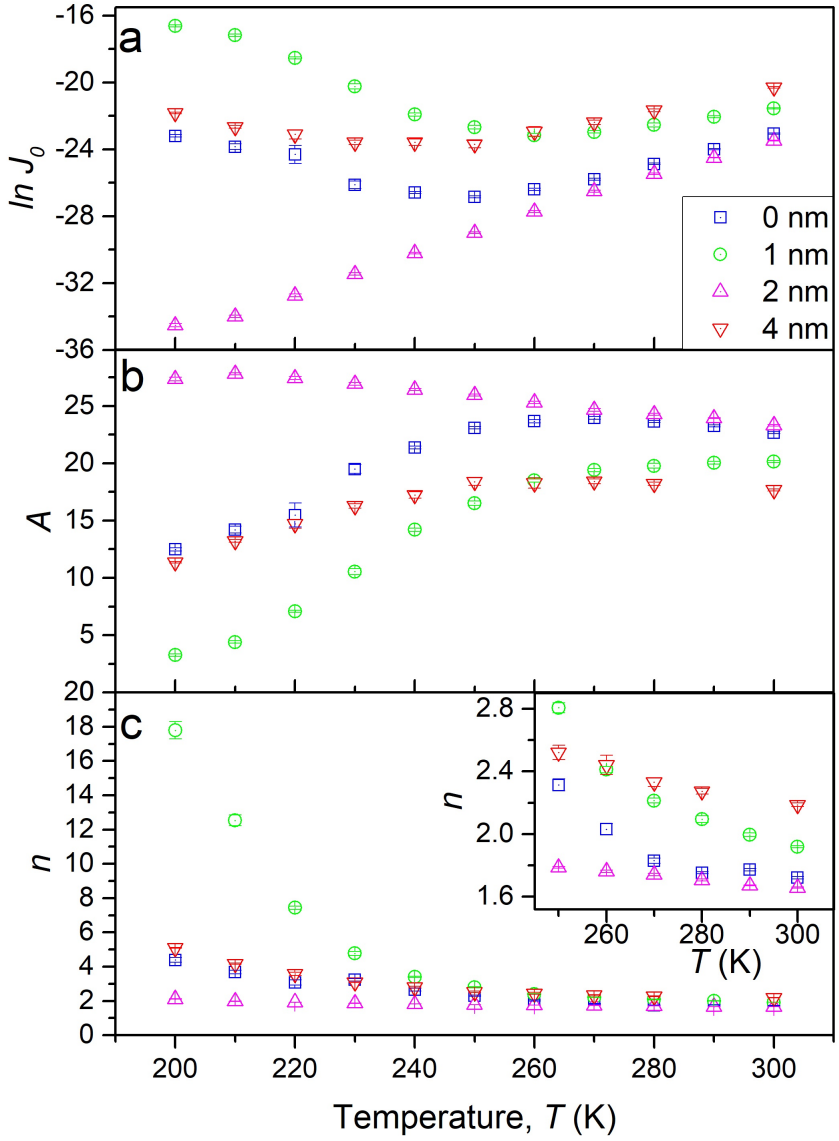

Figure 7.4: Data from $J-V-T$ studies on for CdS/CdTe devices with varying thicknesses of copper in the contacts (Series 721) showing the temperature dependent behaviour of a) $ln\, J_0$, b) slope parameter A and c) n.

Sample	**Cu width** (nm)	N_{nA} (10^{14} cm^{-3})	**Forward bias**		**Reverse bias**			**Back contact**		
			A 300 K	n 300 K	R 300 K	N_t 300 K (cm^{-3})	$\Delta m/\Delta T$ 250-300 K	R_s **calculation**	ϕ_b (eV)	**Fit eq**
721/1	0	1.2	22.7	1.7	8,000	4.5×10^7	-0.01	Slope	0.353 ± 0.002	3.3
721/2	1	0.5	20.1	1.9	25,000	6.3×10^8	-5×10^{-5}	Slope	0.353 ± 0.006	5.1
721/3	2	0.2	23.3	1.7	48,000	8.5×10^6	-0.03	Slope	0.272 ± 0.014	5.1
721/4	4	0.3	17.7	2.2	63,000	1.8×10^9	-6×10^{-4}	Single diode	0.201 ± 0.020	5.1

Table 7.3: The results of analysing $J-V-T$ data for CdS/CdTe devices with varying thicknesses of copper in the contacts (Series 721). The table includes calculated values of slope, A, diode factor, n, and number of tunnelling steps R, which are all calculated from the forward bias data using the multi-step tunnelling model. The reverse bias $J-V-T$ data was used to calculate the trap density, N_t and the exponent m, which can be used to confirm a finding of multi-step tunnelling. N_{nA} was calculated from $C-V$ analysis and will be discussed in the next section. The calculated values for the back contact barrier height, ϕ_b, used either the 'slope' method (section 3.2.3) or fitting to the 'single diode' equation (3.4) to calculate R_S, and which equation was use to calculate ϕ_b. In each case the equation chosen produced the best fit as measured through χ^2 and adjusted R^2. Where not stated, calculated errors for all parameters are less than 5%.

SRH recombination has been reported as the dominant transport mechanism in some devices intentionally doped with copper [10–12]. Although no evidence has been demonstrated here to suggest SRH recombination in Series 721, the discrepancy between the calculated values of n between analysis using equations B.1 and 3.4 for the 4 nm sample may indicate that other mechanisms may be at work in this sample. However, in the absence of illuminated $J-V-T$ data this can not be further investigated.

These findings imply that the multi-step tunnelling model is likely to be the dominant transport mechanism for these devices at room temperature. The number of tunnelling steps R increased with the thickness of the Cu layer.

b) Back contact

The results for back contact barrier height ϕ_b are shown in table 7.3. The value reduced from ~ 0.35 eV in the sample without additional copper, to 0.20 eV in the sample with 4 nm copper (or $\phi_b = (0.227 \pm 0.009)$eV using equation B.1). These values are generally lower than seen in literature. The trend of decreasing ϕ_b with increasing concentrations of Cu appeared clear however, which is consistent with other reports [1, 13].

7.3.1.3 Shallow and deep levels

a) Shallow levels

Mott-Schottky plots and doping density profiles for Series 721 are displayed in figure 7.5 a) and b) respectively. The capacitance of the samples decreases to a minimum in the 2 nm sample, before increasing slightly in the 4 nm sample. The doping profile shows more consistently high values of N_{nA} for the device *without* additional copper, with the best performing device (Cu of 2 nm) having the lowest doping.

The calculated values of N_{nA}, W_D, V_{bi} are shown in figure 7.6. As expected from the doping profile, the value of N_{nA} dropped an order of magnitude from $> 1 \times 10^{14}\,\mathrm{cm}^{-3}$ in the Au-only device to $\sim 2 \times 10^{13}\,\mathrm{cm}^{-3}$ in the 2 nm sample. The unfeasibly large depletion width of $> 4.5\,\mu$m (slightly thicker than the sample) suggests the data is likely to have a large associated error, although the values for V_{bi} are in the expected range.

Despite the unlikely values for W_D, the acceptor density results are consistent with literature values, with many reports of shallow doping in the 10^{13} - $10^{15}\,\mathrm{cm}^{-3}$ range [4, 13, 14]. Suggested explanations for this apparent reduction in doping density include compensation by deep donors towards the CdS/CdTe interface. However there are other possibilities, such as Cu accumulation at grain boundaries

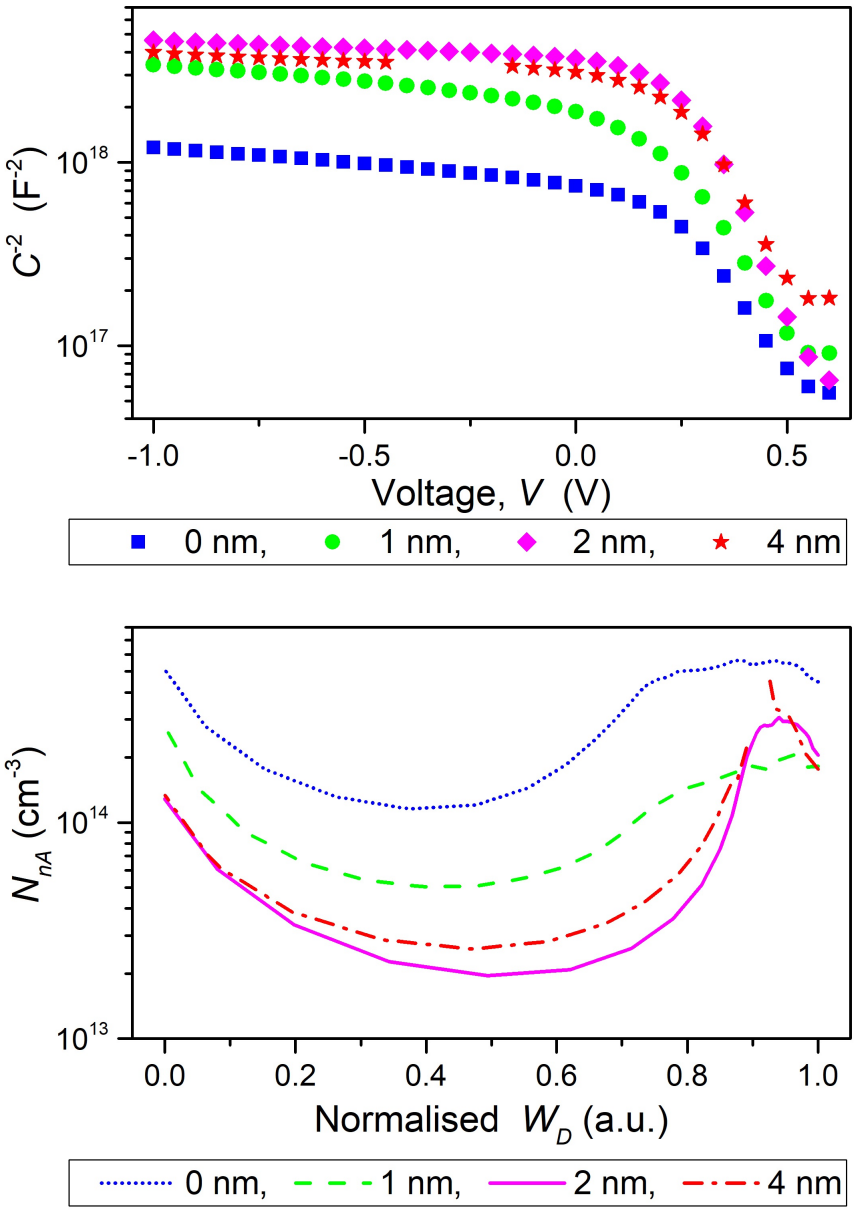

Figure 7.5: Results from $C-V$ analysis on CdS/CdTe devices with varying thicknesses of copper in the contacts (Series 721); a) Mott-Schottky plots, and b) apparent doping density vs normalised depletion width.

[15] and diffusion of Cu to the CdS layer [6]. This latter effect would increase the doping in the CdS layer, and act to increase the depletion width in the CdTe, which could explain the trend seen in figure 7.6 b).

b) Deep levels

Deep level parameters as established through TAS are shown in figure 7.7 and indicated only one trap in each sample. Although the trap levels for 0 nm) and 1 nm of Cu were comparable to the contact barrier height energies, those for

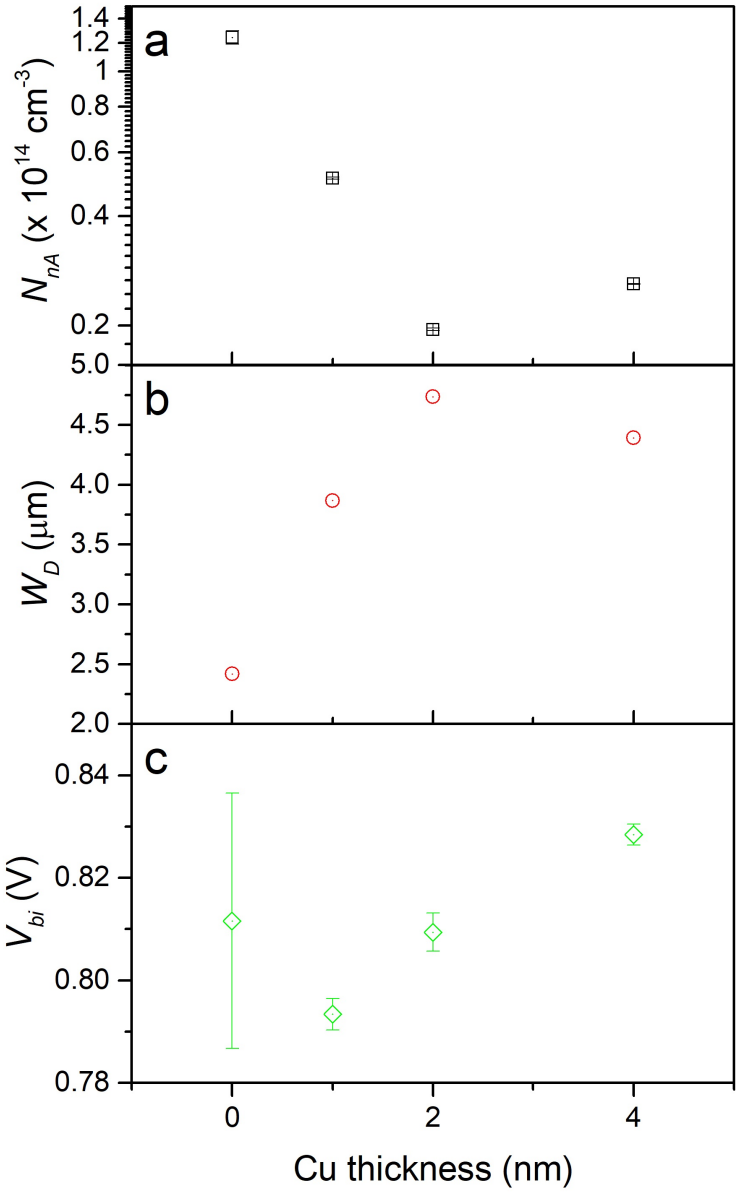

Figure 7.6: Values calculated from $C-V$ analysis of CdS/CdTe devices with varying thicknesses of copper in the contacts (Series 721); a) apparent acceptor density, b) depletion width, and c) built-in voltage.

2 and 4 nm differed greatly and the energies were therefore considered to be due to traps as before. The energy and capture cross-section values are also consistent with traps reported elsewhere for copper-doped CdS/CdTe devices [14]. For the best-performing sample (2 nm of Cu), a trap was evident with an activation energy of (0.205 ± 0.016) eV. There are two traps in this range that are reported in CdTe devices, a cadmium vacancy V_{Cd} (-/2-) (0.21 eV), and a substitutional copper Cu_{Cd} (0/-) (0.22 eV), the latter defect being a commonly reported acceptor [16, 17].

The ~0.35 eV trap seen in the 0 and 1 nm samples could possibly be a Cu-

related deep acceptor, and has been reported in copper containing $CdCl_2$ treated cells [14, 18, 19]. However the trap density for 0 nm (no intentional Cu) was double that of the 1 nm sample, whereas other literature reports have found the trap density to increase with copper concentration.

The 4 nm Cu devices demonstrated a shallower trap at ~0.10 eV which had a very low cross section and moderate trap density. It may be the singly ionised cadmium vacancy V_{Cd} (0/-) (E_A =0.13 eV) or the chloride A-centre complex (V_{Cd}^{2-}+Cl_{Te}^{+}) [2]. (Arrhenius plots from these samples were also partly anomalous, displaying positive rather than negative slopes, as seen by Proskuryakov *et al* for some CdTe devices [20]. However there is not a satisfactory physical interpretation for this at present.)

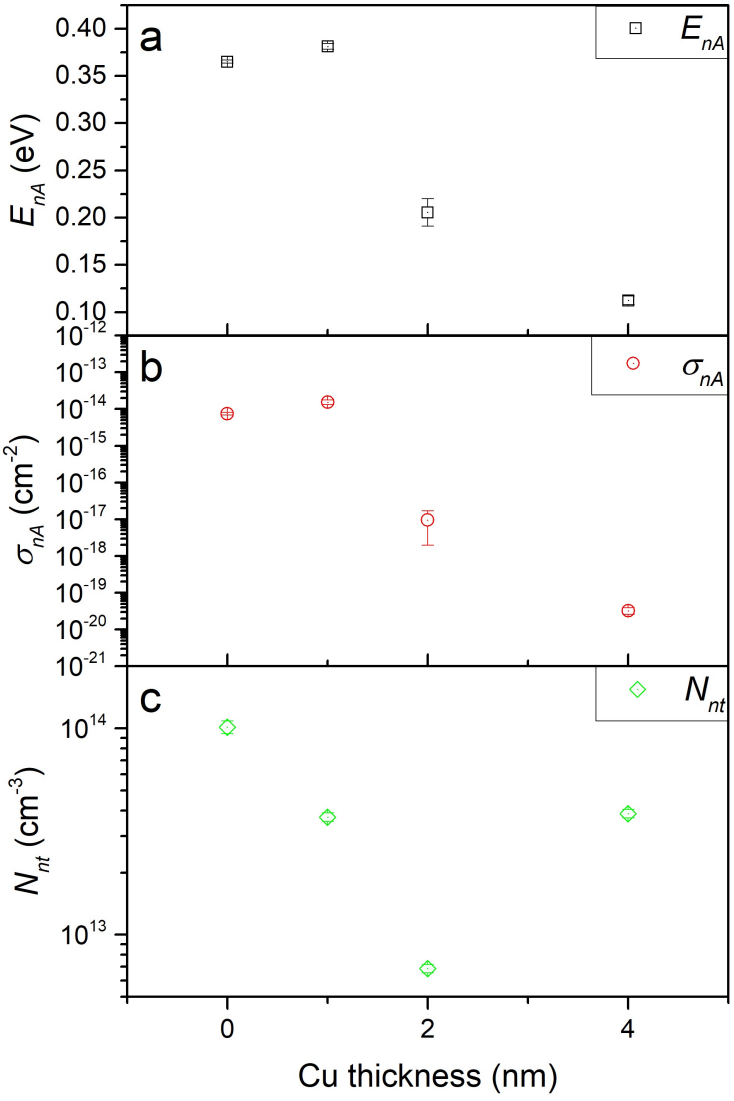

Figure 7.7: Deep trap data for CdS/CdTe devices with varying thicknesses of copper in the contacts (Series 721) calculated using TAS; a) activation energy, b) capture cross section, and c) trap density.

7.3.1.4 Equivalent circuit

The frequency response of admittance data for Series 721 was analysed using equivalent circuit methodology. In figure 7.8 the fit qualities for circuit models 'a' - 'g' (see section 4.3.4.3)are shown. Although it was possible to achieve more fits with the 0 V bias data, better quality fits were possible at 0.6 V, with model 'c' producing more high quality fits than any other circuit, and some trends in component values became apparent. The R_S reduced to a minimum in the sample with 2 nm of copper at the back contact, before appearing to increase in the 4 nm sample. Alongside this the capacitance $C1$ steadily reduced an order of magnitude from 4 to 0.4 nF between the 0 and 4 nm devices, while the CPE became slightly more resistive in nature.

The action of copper to initially reduce the R_S is in keeping with reported

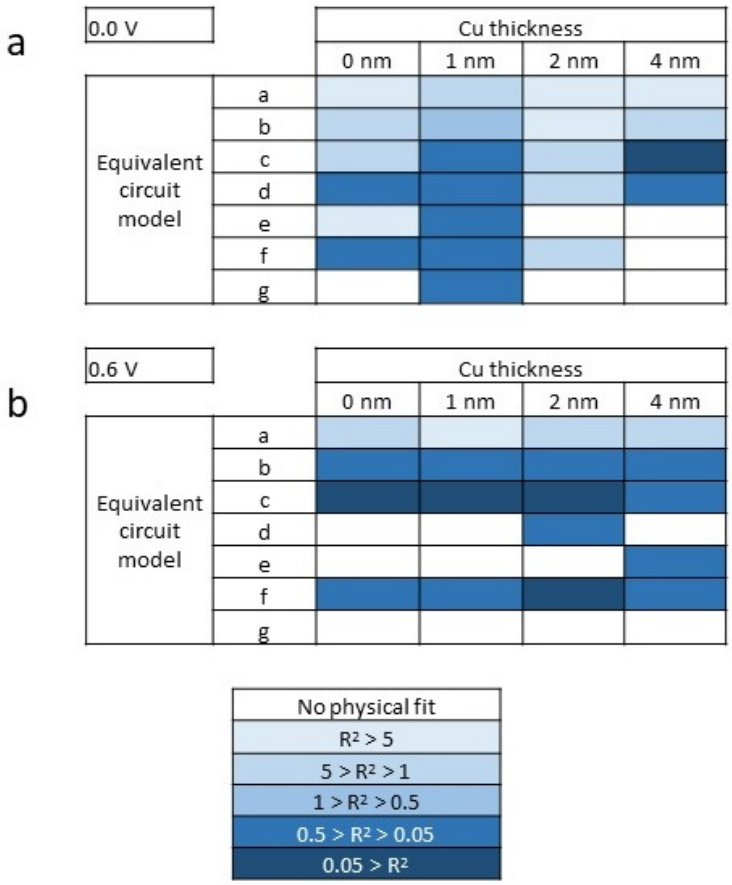

Figure 7.8: A schematic for CdS/CdTe devices with varying thicknesses of copper in the contacts (Series 721) to show the range of fit quality for equivalent circuit models a-g (see figure 4.3) to admittance data at a) 0 V and b) 0.6 V. The fit quality is indicated by a colour guide corresponding to the sum of the squares between the data and the fit. Fits which do not converge, or which provide unphysical circuit components are shown in white.

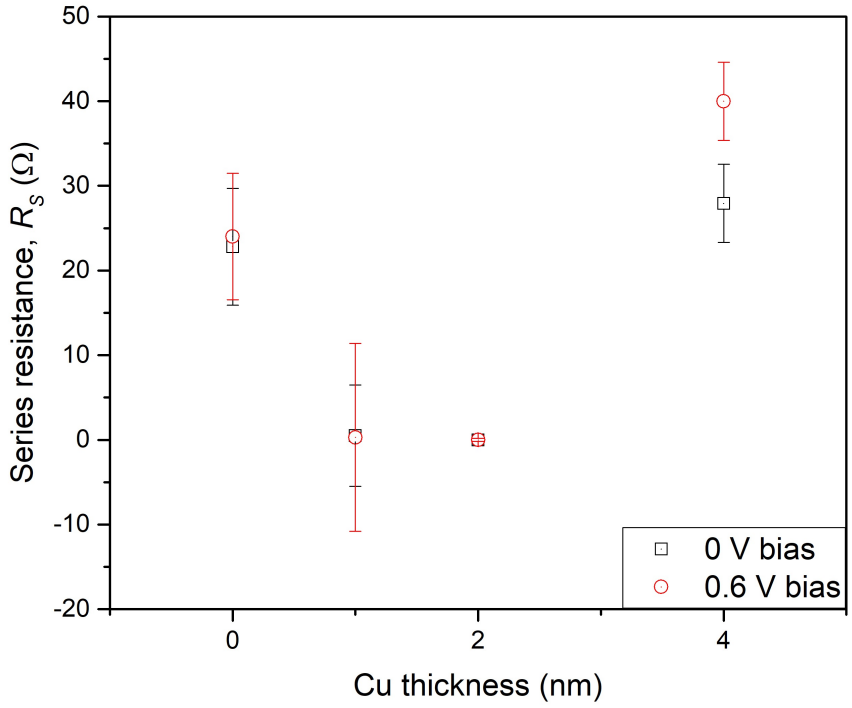

Figure 7.9: Calculated values of R_S from fitting using circuit model 'c' for CdS/CdTe devices with varying thicknesses of copper in the contacts (Series 721), using frequency response admittance data taken at bias voltages of 0 and 0.6 V.

findings [3,21]. The increase in R_S seen in the 4 nm sample is thought to be related to diffusion of Cu to the CdS layer, where it causes deep states and increases this layer's resistivity [22].

7.3.1.5 Summary of results

The findings from analysis of Series 721 are summarised below.

- The addition of a thin layer of copper to the back contact of a CdS/CdTe device processed with $MgCl_2$ acted to increase efficiency and V_{OC}. Back contact barrier height was also reduced.
- Multi-step tunnelling was observed to be the dominant transport mechanism, with the number of tunnelling steps increasing with copper concentration.
- Uncompensated shallow doping density appeared to decrease in copper treated samples.
- The impact of copper on deep trap levels was unclear, with anomalous behaviour (positive Arrhenius slopes) seen in TAS with excess copper.

- Equivalent circuit modelling in forward bias can be fitted well using a circuit consisting of a parallel RC component, a parallel $R-CPE$ component, and a resistance in series (circuit 'c' in section 4.3.4.3).

7.3.2 Back contacts with copper thiocyanate

7.3.2.1 Performance

a) Efficiency and working parameters

Performance data for Series 722 can be seen in figure 7.10. Sample 722/1 and 722/2 were manufactured using n-propyl sulphide (n-PS) as the CuSCN solvent, whereas diethyl sulphide (DES) was used for 722/3 and 722/4. The efficiency of the devices varied with solvent, and the solution concentration - the weaker solution ($2\,\mathrm{mg\,ml^{-1}}$) produced higher efficiency for both solvents (722/1 and 722/3) than the higher concentration solution ($50\,\mathrm{mg\,ml^{-1}}$ used for 722/2 and 722/4). Although the best performing sample plate, 722/1, had a high average efficiency, with a range from 12 - 13.5%, sample 722/3 had a slightly lower average efficiency

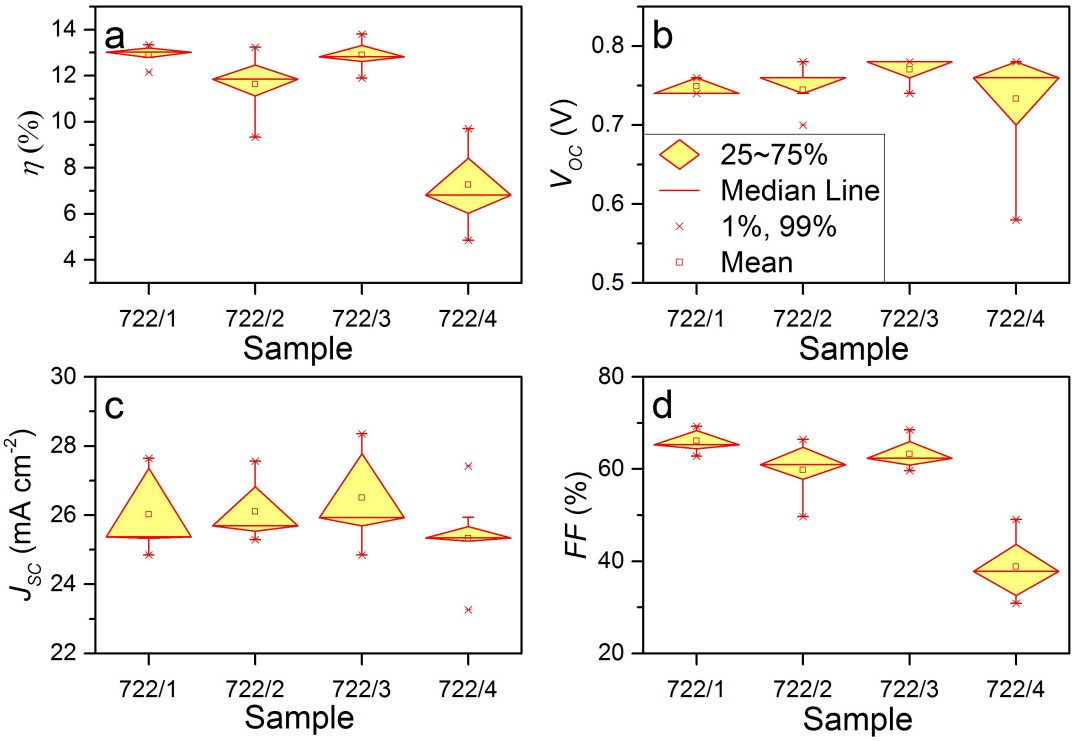

Figure 7.10: Box plots demonstrating the spread of performance parameters for CdS/CdTe devices with a CuSCN layer at the back contact (Series 722): a) efficiency, b) open-circuit voltage, c) short-circuit current density and d) fill factor. There were N contact dots per sample plate (Max $N = 9$).

despite a higher mean V_{OC} and J_{SC}. Sample 722/4 had a lower value of η than the rest of the series, largely attributable to a halving of the mean FF.

The $J-V$ curves shown in figure 7.11 are very similar for the three sample sets 722/1-3, with high R_{SH}, low R_S, turn-on voltage $\sim 0.6\,\mathrm{V}$, and no apparent roll-over in forward bias. In comparison a significant deterioration was evident in sample 722/4: R_{SH} was decreased, R_S increased, turn-on voltage $< 0.5\,\mathrm{V}$, and roll-over evident.

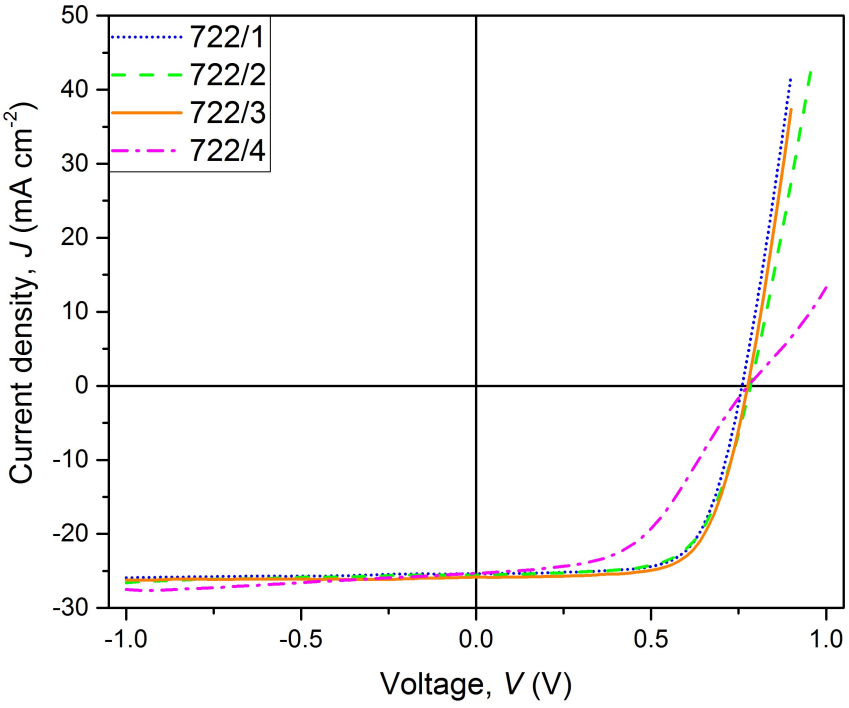

Figure 7.11: Typical $J-V$ curves for CdS/CdTe devices with a CuSCN layer at the back contact (Series 722).

From the performance data of Series 722 it appears that in excess, CuSCN causes deterioration in device performance. However all sample plates had excellent mean values for V_{OC} and J_{SC}, at $> 0.74\,\mathrm{V}$ and $> 25\,\mathrm{mA\,cm^{-2}}$ respectively.

b) EQE

Figure 7.12 contains EQE data for Series 722 devices - all are similar. Above 550 nm there is a small difference in EQE evident between the two solvent types, with the DES processed devices (722/3,4) showing slightly greater efficiency than the n-PS devices (722/1,2). This slight increase may be an indication of reduced recombination, or increased depletion width allowing for improved collection of the longer wavelength photons.

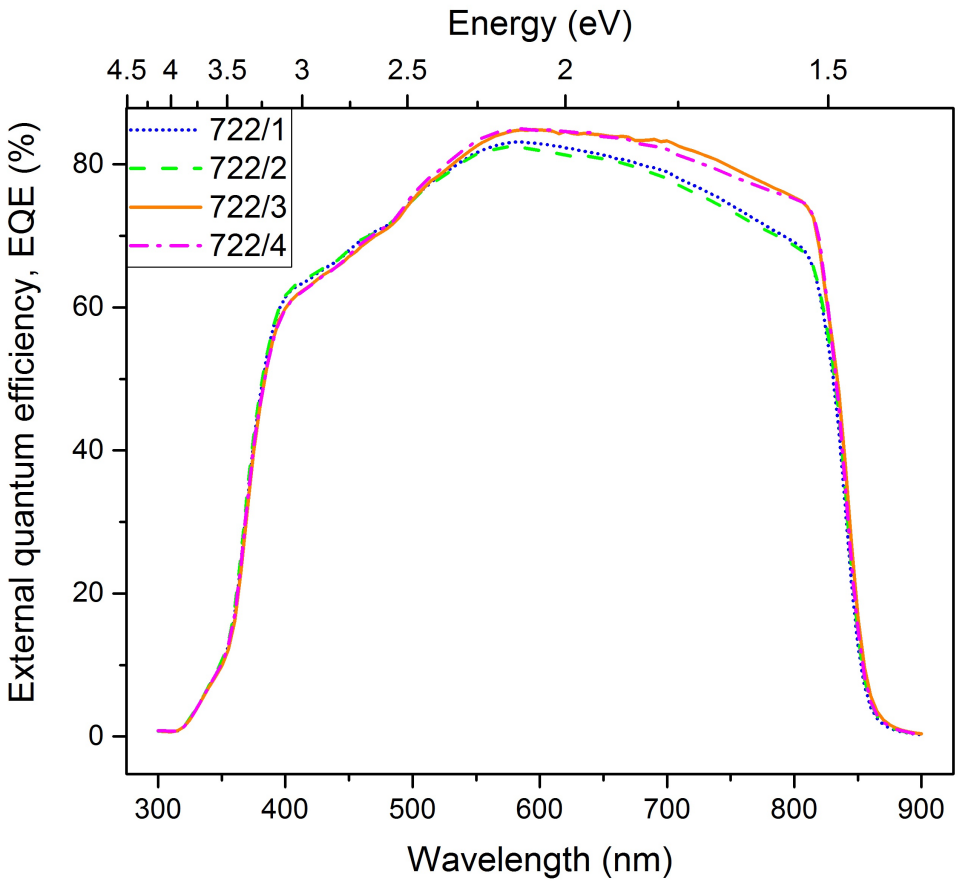

Figure 7.12: Typical EQE curves for CdS/CdTe devices with a CuSCN layer at the back contact (Series 722).

7.3.2.2 Current transport

a) Main junction

Data from $J-V-T$ studies on Series 722 is shown in figure 7.13, which showed the temperature dependence of $ln\, J_0$, A, and n. The main features are;

i. All samples had appropriate temperature dependence of $ln\, J_0$ with T above 230 K, below which the multi-step tunnelling model failed.

ii. A was approximately invariant above 250 K.

iii. Atypically for the multi-step tunnelling model, all samples displayed an invariance of n with T above 250 K.

iv. When analysed for features of recombination in the depletion region all samples were found to obey $ln\, J_0 \propto -1/T$ above 250 K, but none satisfied the equality $n\Delta E = V_{bi}$, ruling out this transport mechanism.

When analysed in reverse bias, all four sample plates showed evidence of multi-step tunnelling, with a negative slope of $\Delta m/\Delta T$ confirming the dominant

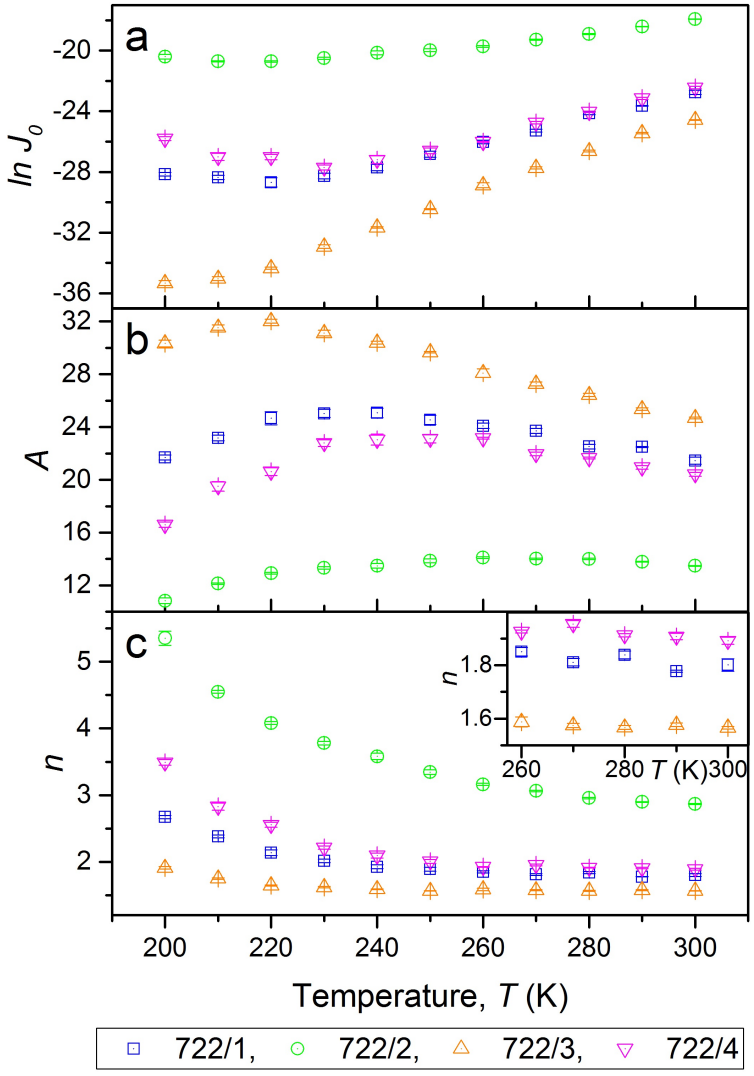

Figure 7.13: Data from $J-V-T$ studies on CdS/CdTe devices with a CuSCN layer at the back contact (Series 722) showing the temperature dependent behaviour of a) $ln\, J_0$, b) slope parameter A and c) n.

Sample	**Solvent**	**Conc.** ($\mathrm{mg\,ml^{-1}}$)	$\boldsymbol{N_{nA}}$ (10^{14} $\mathrm{cm^{-3}}$)	**Forward bias**		**Reverse bias**			**Back contact**		
				$\boldsymbol{A}$ 300 K	$\boldsymbol{n}$ 300 K	$\boldsymbol{R}$ 300 K	$\boldsymbol{N_t}$ 300 K ($\mathrm{cm^{-3}}$)	$\boldsymbol{\Delta m/\Delta T}$ 250-300 K	$\boldsymbol{R_s}$ **calculation**	$\boldsymbol{\phi_b}$ (eV)	**Fit eq**
722/1	n-PS	2	2.7	21.4	1.8	4,000	3.8×10^{9}	-8×10^{-4}	Slope	0.303 ± 0.002	3.3
722/2	n-PS	50	2.9	13.4	2.9	9,600	6.6×10^{8}	-3×10^{-3}	Slope	0.303 ± 0.003	3.3
722/3	DES	2	0.7	23.7	1.6	12,000	7.2×10^{8}	-0.01	Slope	0.382 ± 0.005	3.3
722/4	DES	50	0.9	20.4	1.9	13,000	1.1×10^{9}	-4×10^{-3}	Slope	0.323 ± 0.002	3.3

Table 7.4: The results of analysing $J-V-T$ data for CdS/CdTe devices with a CuSCN layer at the back contact (Series 722). The table includes calculated values of slope, A, diode factor, n, and number of tunnelling steps R, which are all calculated from the forward bias data using the multi-step tunnelling model. The reverse bias $J-V-T$ data was used to calculate the trap density, N_t and the exponent m, which can be used to confirm a finding of multi-step tunnelling. N_{nA} was calculated from $C-V$ analysis and will be discussed in the next section. The calculated values for the back contact barrier height, ϕ_b, used either the 'slope' method (section 3.2.3) or fitting to the 'single diode' equation (3.4) to calculate R_S, and which equation was use to calculate ϕ_b. In each case the equation chosen produced the best fit as measured through χ^2 and adjusted R^2. Where not stated, calculated errors for all parameters are less than 5%.

transport mechanism. The results from this analysis are included in table 7.4. The number of tunnelling steps R was found to be slightly higher in the samples manufactured using DES, but the trap density N_t was similar for all samples.

b) Back contact

Data from $J-V-T$ studies on Series 722 was used to determine the back contact barrier height, ϕ_b. These results are shown in table 7.4. A difference can be seen between the two solvents used in manufacturing. Both samples created using n-PS (722/1,2)to deposit the CuSCN layer had values of $\phi_b \approx 0.30\,\text{eV}$, whereas the DES samples had higher values, with $\phi_b \approx 0.38\,\text{eV}$ (722/3). Despite the significant different in barrier height, the device performances were rather similar, indicating that moderate barriers do not adversely affect cell performance.

7.3.2.3 Shallow and deep levels

a) Shallow levels

Frequency dependent $C-V$ data was analysed to produce Mott-Schottky and doping density plots as shown in figure 7.14. Samples manufactured with the same solvent had very similar behaviours. In panel a) all four samples appeared almost fully depleted at 0 V bias, with a slope of ~ 0 in the reverse bias region. In panel b) again the curve shape was similar across all samples, with a region of high doping ($N_{nA} > 10^{16}\text{cm}^{-3}$) towards $W_D = 1$ (the back contact region [23, 24]) and a comparatively shallow 'U' shape across the bulk of the depletion region. The shallow doping in the bulk was somewhat greater in the samples processed with n-PS, namely 722/1 and 722/2.

The calculated parameters N_{nA}, W_D and V_{bi} are shown in figure 7.15. As expected from analysis of the Mott-Schottky plots, the shallow doping appears much greater in samples 722/1 and 722/2 than in 722/3 and 722/4, with values of N_{nA} in the DES samples approximately half those seen in those manufactured using n-PS. The solvents used have also affected the depletion width seen in panel b) with the n-PS samples (namely 722/1 and 722/2) demonstrating a smaller value of W_D, although there is little variation in the values of V_{bi} in panel c). This could be indicative of an improved quality junction in these samples. The larger values for W_D seen in the DES samples (722/3 and 722/4) would explain the improved appearance of the EQE curve at long wavelengths (figure 7.12).

b) Deep levels

Frequency response admittance data was analysed using TAS for Series 722. All four samples demonstrated three dispersions in capacitance. The deepest energy

signal was consistent with measured values for ϕ_b, as shown in figure 7.16. It is therefore thought that in this case TAS is measuring back contact barrier height, and this data is not included in the following analysis of deep levels.

Trap level data in figure 7.17 shows the values for E_{nA}, σ_{nA}, and N_{nt}. All

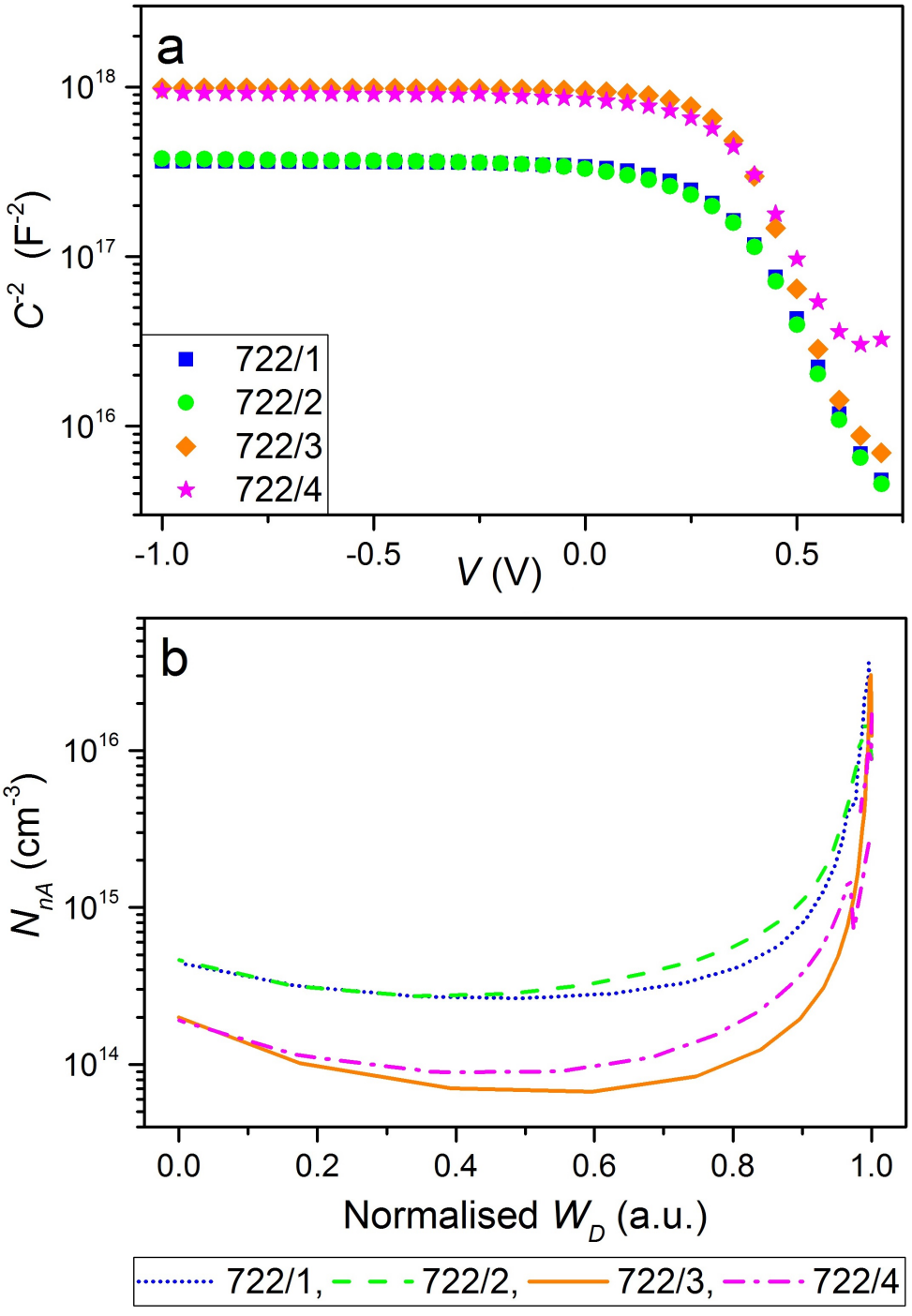

Figure 7.14: Results from $C-V$ analysis on CdS/CdTe devices with a CuSCN layer at the back contact (Series 722); a) Mott-Schottky plots, and b) apparent doping density vs normalised depletion width. Samples 722/1&2 were made using n-PS solvent while 722/3&4 were made with DES solvent - the differences may result from the differing solubility of CuSCN in these solvents.

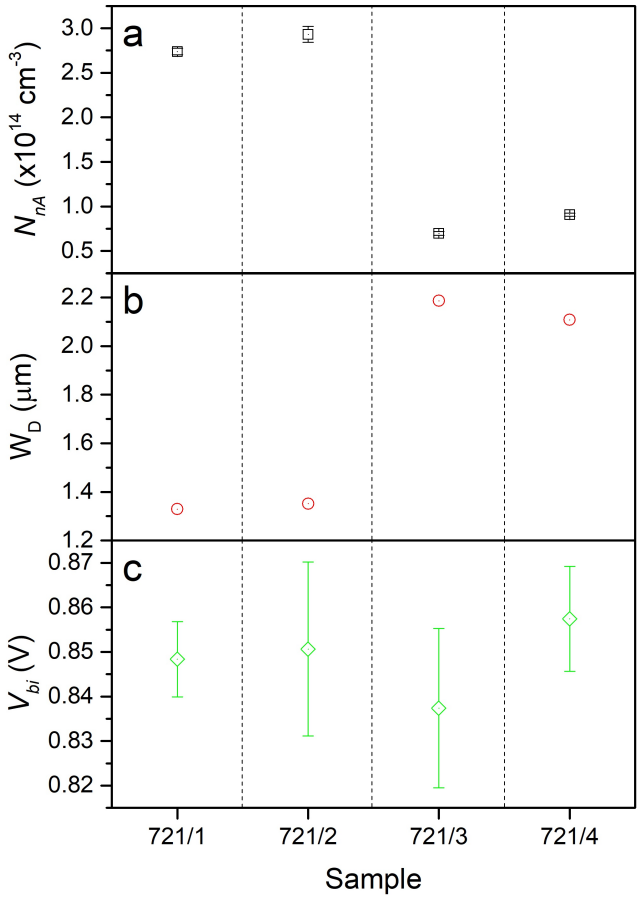

Figure 7.15: Values calculated from $C-V$ analysis of CdS/CdTe devices with a CuSCN layer at the back contact (Series 722); a) apparent acceptor density, b) depletion width, and c) built-in voltage.

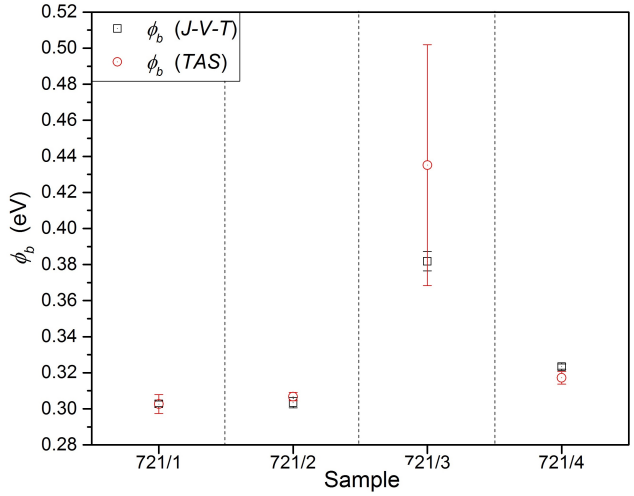

Figure 7.16: A comparison of ϕ_b calculated from $J-V-T$ data and TAS for CdS/CdTe devices with a CuSCN layer at the back contact (Series 722), and a trap level extracted from TAS data.

samples demonstrated a shallow trap in the range 0.05 - 0.08 eV, and a slightly deeper trap between 0.100 - 0.135 eV. On comparison of samples 721/1 and 721/3, the only significant difference was the energy and trap density of the shallow level, which in sample 721/3 had the lowest activation of the four sample plates. This trap increased in density in the samples manufactured with more concentrated solution (samples 722/2 and 722/4) which may indicate it was related to CuSCN concentration. In contrast, the deeper trap reduced in trap density in these samples.

The deeper of the two observed traps is likely to be related to either the cadmium vacancy defect V_{Cd} (0/-) 0.13 eV, or the (V_{Cd}^{2-}+Cl_{Te}^{+}) acceptor defect. Traps of this energy have been observed in CdTe elsewhere (including $MgCl_2$ processed devices) [18, 25–28]. The shallower trap however is perhaps more interesting. Although traps of this energy observed elsewhere in high-purity have been attributed to impurities of N, Na, P, As and As CdTe [16, 27–30], their presence

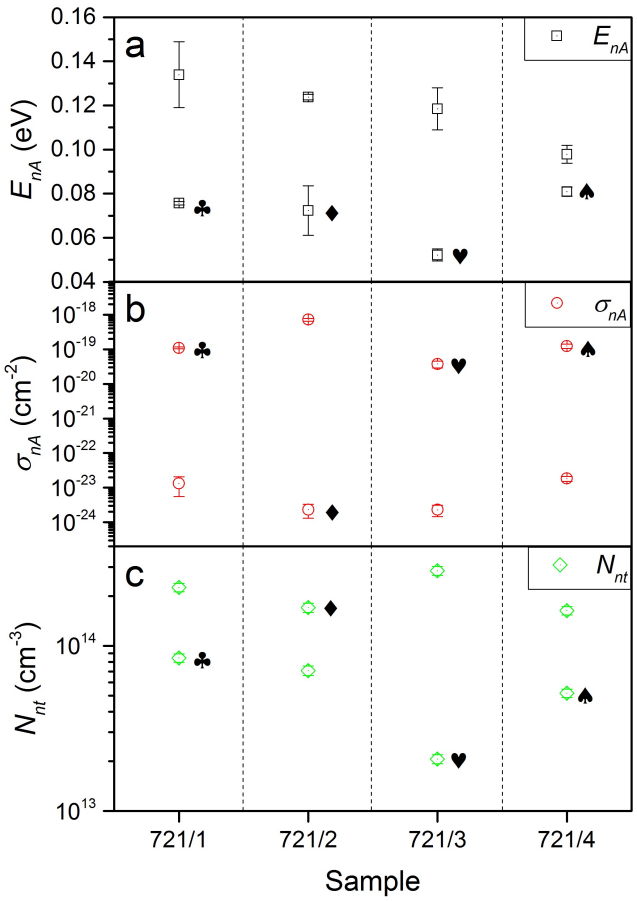

Figure 7.17: Deep level data for CdS/CdTe devices with a CuSCN layer at the back contact (Series 722) calculated using TAS; a) activation energy, b) capture cross section, and c) trap density. Where there are multiple traps, the black symbols allow correlation between vertical panels.

in all samples in this series could indicate a nitrogen shallow acceptor state. This raises the possibility that the thiocyanate layer may be doping the CdTe with nitrogen (although the defect formation energy of N_{Te} is large, and the nitrogen is covalently bonded to carbon in CuSCN).

7.3.2.4 Equivalent circuit

The fit quality for equivalent circuit models 'a' to 'g' (see section ch:exp:eca) is shown in table 7.18. At neutral bias almost all models could produce a physical fit, but only model 'c' permitted low R^2 values at both 0 and 0.6 V. However for samples 722/1 and 722/3, no fit was possible with $R^2 < 0.05$ at either bias, suggesting that none of these circuits precisely described these devices.

Using circuit model 'c', the calculated values for R_S are shown in figure 7.19. These resistances are very low in all samples with the exception of 722/4, the $J-V$ curve of which was noted to have greater series resistance (figure 7.11).

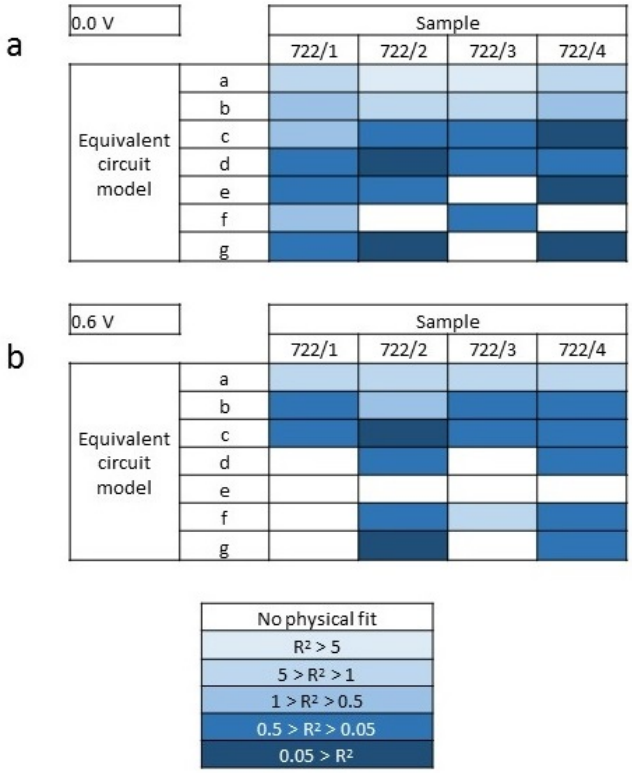

Figure 7.18: A schematic for CdS/CdTe devices with a CuSCN layer at the back contact (Series 722) to show the range of fit quality for equivalent circuit models a-g (see figure 4.3) to admittance data at a) 0 V and b) 0.6 V. The fit quality is indicated by a colour guide corresponding to the sum of the squares between the data and the fit. Fits which do not converge, or which provide unphysical circuit components are shown in white.

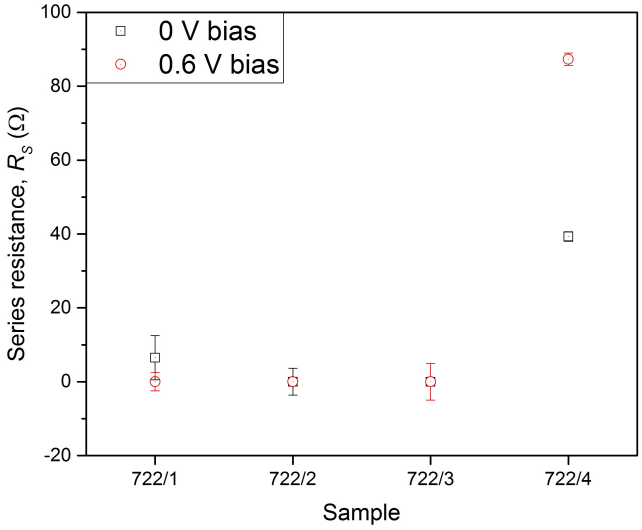

Figure 7.19: Calculated values of R_S from fitting using circuit model 'c' for CdS/CdTe devices with a CuSCN layer at the back contact (Series 722), using frequency response admittance data taken at bias voltages of 0 and 0.6 V.

7.3.2.5 Summary of results

The findings from analysis of Series 722 are listed below.

- The use of CuSCN at the back contact of CdS/CdTe devices has produced high efficiency devices (~13%) with high values of V_{OC} (~780 mV) and J_{SC} (~26 mA cm^{-2}).
- The devices demonstrated excellent $J-V$ curves with high R_{SH}, low R_S and high turn-on voltage, with no evidence of roll-over. Excess CuSCN (from spin coating in high concentrations) appeared to be detrimental to device performance, increasing R_S and roll-over.
- The solvent used to form the thiocyanate layer appeared to cause changes in the electrical parameters of the finished devices, although these differences could be related to the relative solubility of CuSCN, and the resulting layer thickness.
- Multi-step tunnelling was found to be the dominant transport mechanism for all samples. The back contact barrier height was lower than normally seen in these devices (0.3-0.38 eV compared to 0.40 - 0.56 eV).
- Doping profiles showed high shallow acceptor concentration at the back contact and comparative homogeneity across the depletion width, with fully depleted devices from $C-V$ analysis.

- Equivalent circuit modelling of the AC response was best fitted to model 'c' (section 4.3.4.3), containing an $R-C$ segment, $R-CPE$ component and a series resistance.

7.3.3 Discussion

Back contact barrier

As discussed in chapter 2, one of the fundamental difficulties with the use of CdTe in photovoltaic devices is the difficulty of finding materials that have sufficiently high work functions to create an Ohmic contact. As such, when using metals such as gold, a Schottky barrier is formed, impeding the transport of holes in particular. Carriers are able to cross the barrier by tunnelling, thermionic emission, or a combination of the two. By increasing the doping near the back contact, the number of carriers crossing the barrier is increased. Several techniques are already used to try to perform exactly this task, for example chemical etching before application of the contact increases the local doping, reducing the depletion width allowing more charge carriers to cross.

In this chapter, two methods of minimising the effect of the Schottky contact have been studied. It has been shown that neither Cu nor CuSCN layers at the back contact overcome the fundamental barrier height, and the junction is always rectifying. However, there is evidence to suggest that they reduce both the 'effective barrier', and R_S, and this is consistent with literature reports [3, 21]. The limited study of CuSCN presented here has demonstrated possible advantages over Cu alone, with higher performance parameters, potentially improved junction formation and possible higher stability although further studies would be required to confirm this statistically.

Doping

Like other wide band-gap II-VI semiconductors, doping of CdTe has proven to be problematic and has been extensively researched [31]. Compensation mechanisms are widely thought to counteract additional acceptor doping [32], with hole densities thought to be several orders of magnitude less than the acceptor density [33]. Copper diffuses readily through CdTe, and there is evidence of Cu migration to grain boundaries to passivate Te dangling bonds [7, 15, 34, 35]. The local Cd lattice content affects the chemical potential to influence the formation of Cu_i or Cu_{Cd} vacancies, creating a narrow window where the addition of Cu improves the hole density. It has been reported that over-treatment with copper acts to reduces carrier lifetimes, and eventually would make CdTe insulating or

n-type [5, 11, 25]. The analysis of Series 721 (with varied Cu) has demonstrated apparent reductions in shallow doping even as device performance improved, with a local minimum in R_S in an optimised sample. On the contrary, the use of copper thiocyanate in Series 722 caused an increase in acceptor density, with a concomitant reduction in R_S producing high values of V_{OC} and J_{SC}. It is speculated that the copper may diffuse less when applied as a part of this salt, acting to increase the local doping around the back contact.

7.4 Implications for improving cell performance

Copper doping is frequently used to improve the efficiency of CdTe device. However over-treatment can act to reduce cell performance. The high mobility of Cu ions can result in migration to the CdS layer, which is undesirable, and eventually catastrophic for the device. The studies in this chapter suggest that a stable Cu-containing salt may reduce the movement of Cu throughout the layers of the cell, providing high doping at the back contact allowing for improved performance.

7.5 Conclusion

The use of copper thiocyanate at the back contact of CdS/CdTe devices may provide a stable alternative to Cu. Further work would include a larger study of devices to establish statistical reliability and to investigate the effects of varying the amount of CuSCN. SIMS analysis would be interesting, to assess whether the thiocyanate prevents Cu diffusing through the CdTe layer into the CdS window. In a similar vein, studying long term stability of devices under working conditions would be useful to demonstrate any advantages over other sources of copper doping.

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8. Discussion

This section provides further discussion of a) appraisal of the experimental methodologies, reproducibility and systematic error (8.1), b) the relationships between point defects, the contact barrier, and processing (8.2), and c) factors that affect V_{OC} (8.3).

8.1 Evaluation of the experimental methodology

Materials uniformity and variability

For small scale lab manufacture of research solar cell devices, reproducibility and uniformity are expected to be very much lower than for individual processes. Typically for a given sample plate having 9 contact dots of (0.25 x 0.25) cm^2 area the working parameters and their standard deviations were as follows;

Parameter	**Mean**	**Error**
η (%)	5.60	0.16
V_{OC} (mV)	651	6
J_{SC} ($mA\,cm^{-2}$)	14.5	0.3
FF (%)	57.1	0.9

Table 8.1: The mean efficiency and standard deviation of the mean for 9 contact dots on a sample plate.

Meanwhile there was run-to-run variability also with repeats of the same growth conditions giving different outcomes (for example the as-grown CdS samples from Series 521 and 622 [sample plates 521/1 and 622/34]). Generally the approach in sample manufacture was to minimise the effects of variations by a) making up to 9 contact dots on each piece of material so as to provide averages, b) conducting series of runs with a systematically adjusted variable, such that

trends were able to verify the self-consistency of the data set, and c) making all the devices from a series on a back-to-back set of growth/processing runs so as to avoid the influence of drift of the baseline conditions. In addition to this it was found that the somewhat extreme temperature cycles endured by the samples during electrical measurements occasionally had a profound effect on the samples and could act to irreversibly degrade them.

The underlying causes of these effects are now discussed;

Possible causes of variation within a series

i. Statistical variation in number of pinholes in the window layer causing shunted devices, changing the number of functioning cells on a sample plate (N). This can be affected by the thickness of the window layer, with thicker windows producing less pinholes.

ii. Changes in the thickness of layers across each sample plate, potentially affecting the optical properties (see figure 4.1: the window layer was deposited on a rotating [5 x 5] cm sample which was then broken into quarters, before CSS CdTe deposition on the static sample). The layer uniformity of sputtered, CSS, and spin coated materials is likely to vary across each sample plate through geometric factors, and although techniques such as rotating the sample may help, they are not practical for CSS for example. However, the size of the sample plates and the contact placement onto each plate is designed such that, through symmetry, each part of the plate is similarly tested. To investigate the possibility of systematic error in devices with relation to their position on a sample plate, all the sample plates investigated in this work were compared statistically. While the Student t test showed no significant variance in the mean efficiency of central, corner or edge cells, a Pearson's chi-squared test demonstrated that low efficiency devices ($\eta < 1\%$) were not likely to have a normal distribution across the sample plate, with devices on the corners appearing more likely to have $\eta < 1\%$ than central devices (p=0.014). However, there was no statistically significant difference between each corner, and no evidence of parameters V_{OC}, J_{SC} or FF being dependent on the device position on the sample plate. (High efficiency cells and performance parameters appeared to be normally distributed across the sample plate.) It is therefore thought that despite the variation across the plates, the systematic error would be present for all sample plates, so they remain self-consistent within each sample series.

iii. Area of collection effect from outside contact area. As collection from the edges of contacts can increase the apparent J_{SC}, it is conceivable that devices towards the edge of a sample plate may have lower performance than in the centre (although this effect is likely to be small, as etched CdTe has a high sheet resistance ($\sim 0.5\,\mathrm{M\Omega\square}$) [1]).

Variation between series

i. Changes to the CdTe source potentially affecting stoichiometry and oxygen content during growth. This cannot easily be quantified. Variation in the thermal history from run to run, and hence affects on sulphur diffusion (including consumption of the CdS layer) and variations in the thin film chemistry which would effect the local Fermi level [2–5].

ii. baseline drift e.g. from gradual changes of the source and chamber conditioning.

Reproducibility of electrical measurements

i. For the temperature dependent electrical measurements, performing the same experiment on the same sample twice was more likely to produce different results if the experimental temperature exceeded the range 110-310 K. For TAS and $C-V$ analysis it was not possible to test two contact dots simultaneously, and consecutive experiments on two contacts on the same sample plate usually produced consistent results, but not always. In some of the results, the second contact tested would develop anomalous Arrhenius behaviour, and significant deterioration of $J-V$ curve (whether or not it had been contacted with conductive paste during the first experiment). These changes were similar in devices contacted with graphite- or silver-based adhesive paste and were lessened by containing experiments in the temperature window above. $J-V-T$ studies, conducted on two devices at the same time, produced consistent results, but repeating the experiments on the same samples produced different results. It is thought that the contacting paste damaged the devices from possible in-diffusion of silver, and from thermal expansion leading to de-lamination.

ii. Although the temperature ranges used for TAS and $J-V-T$ experiments were kept identical for all studied series for consistency, changing the temperature range and number of measurements would be useful for future work: for TAS a reading at every 5 K above 190 K would

improve the Arrhenius plot, and changing the $J-V-T$ measurements to readings between 250-300 K, with readings every 5 K to improve data collection for the exponential R_S-related curve while reducing the damaging impact of the heat cycling on the cell.

Analysis of the frequency response data

i. While extraction of data to populate the Arrhenius plot used in TAS is comparatively straightforward, some trap signals were only evident at low amplitude over a narrow temperature range, reducing the number of data points available necessitating the use of the 'overlap' technique as described in section 3.3.3 to provide an estimate of E_nA. This method was used to minimise the error in interpreting noisy data.

ii. For analysis of the TAS signal, it is assumed that σ_{nA} is not temperature dependent, such that the trap signatures seen on Arrhenius plots are linear. However, for some devices, Arrhenius plots appeared slightly curved. It is not known whether this was a measurement artefact, an intersection of two linear trap signatures with similar activation energies, or an indication of a temperature dependence of σ_{nA}. If the latter is the case, the activation energy E_{nA} (an enthalpy) could be very different to the energy separation of the trap from the band edge (a Gibbs free energy) [6]. This systematic error is difficult to quantify.

iii. Analysis of impedance data using the equivalent circuit methodology (see section 4.3.4.3) frequently produced multiple viable solutions, especially when more circuit elements were involved. In these cases the more appropriate circuit was chosen (i.e. more physically viable, closer in relationship to circuit parameters of the same device at a different voltage, or similar to circuits of different devices in same series), but it is possible that other solutions were more representative of the physical device.

While attempts were made to produce consistent samples and experimental data, it is thought the only viable solution to the multiple error sources inherent in this work is to increase the data sets. Meanwhile, the existing data and analysis is likely to have increased reliability when comparing trends of data rather than specific values.

Thermal admittance spectroscopy

The use of TAS in this work has provided evidence of trends of behaviour consistent within each series, but not necessarily across sample sets. In several series, traps were evident in TAS having values consistent with the measured back contact barrier heights, although similar (possible back contact) traps were notably absent in other series. As has been mentioned elsewhere, there have been reports in literature of samples when the back contact has, or has not been observed by TAS [7, 8]. Burgelman and Nollet used the SCAPS software to simulate TAS spectra of CdTe devices. They found that shallow and deep traps gave rise to capacitive signals at high frequency, and low frequency respectively (in different temperature ranges). They argued that the large capacitance decay at mid temperatures and mid frequency frequently observed in CdTe cells could be attributable to an energy contact at a barrier, which could also cause a transient signal on DLTS [9]. The correlation between some trap levels seen in this work and back contact barrier heights has been strong, leading to the conclusion that on some occasions TAS does detect the energy barrier, yet in other samples this is markedly absent. The physical explanation behind this is as yet unclear.

8.2 Experimentally observed behaviours

Equivalent circuit analysis

It has been demonstrated in this work that several equivalent circuit models could provide reasonable fits for impedance data at different voltages. All series did however fit circuit model 'c' best (section 4.3.4.3), which consisted of a parallel $R-C$ component, a parallel $R-CPE$ component and a series resistance R_S. Interestingly, almost all of the Cole-Cole plots (Z' vs Z'') demonstrated only a single semi-circle, with the angle of depression changing at different voltages (indicating a change in CPE values), yet did not fit well with circuit model 'a' (a circuit consisting of a single parallel $R-CPE$ component and a series resistance) with a CPE replacing the capacitor. This may be an indication of the relative importance of the two parallel components, with one having a far greater physical impact on the device than the other. However, circuit model 'c' was not always an excellent fit, and the quality of the fit often changed as a function of voltage bias. This could be understood by considering the bias affect on the device: at 0 V bias, the back contact junction is open (large depletion width) while the front junction (the CdS/CdTe heterojunction) is comparatively closed. At a forward bias of 0.6 V the situation is reversed for most devices, with the back junction closing.

Several cells demonstrated a good fit to circuit 'd' at neutral bias, which was not possible at 0.6 V. Model 'd' has an $R-CPE$ series element in parallel with a second CPE, with a series resistance. It is speculated that the back junction can be modelled by a parallel RC component, which is of far lower electrical significance than the rest of the device. When the back junction is open and the front junction is closed the device output is dominated by the front junction, with the parallel RC component almost negligible. When in forward bias however the back junction dominates, and model 'c' is more appropriate, with the front junction approximating to a parallel $R-CPE$ element. At neutral bias there may be more CPE behaviour evident, with a single parallel junction dominating the device. The presence of the CPEs in this circuit would indicate a spectrum of capacitive and resistive elements, which Proskuryakov *et al* speculated would represent the non-uniform resistance of the $p-n$ junction (the $CPE1-R1$ elements) and the non-uniform capacitance of the $p-n$ junction ($CPE2$) [10]. However it is possible one of these CPE elements is influenced by the grain boundary (GB) behaviour.

For many of the best performing devices the value of R_S in circuit model 'c' was close to zero. It should be noted that this does not imply the DC R_S was also zero, although in some cases this appeared to be the case (the optimised device in Series 521 for example).

It may be possible to further investigate the electrical components of a device by measuring a sample in parallel with a physical equivalent circuit, although simulations would be simpler to implement. Agreement of the data would still not be confirmation of the electrical components however. For devices where the components could be physically separated and measured independently, that approach would prove useful, but cannot feasibly be applied to CdS/CdTe devices. If a parameter could be changed during manufacture or processing which affected only one junction, this variation of this parameter would allow study of the junction. However in these complex materials there are few, if any, parameters which have such a limited area of impact.

$J-V-T$ studies

Throughout this work $J-V-T$ studies have been used to assess the back contact barrier height and the dominant transport mechanisms. The values for back contact barrier height have varied from 0.20 - 0.50 eV (device 721/4, with Cu at back contact, and device 621/4, as-grown CdS:O respectively). Comparable devices from different series were found to have consistent values of ϕ_b increasing confidence in the calculated values and experimental accuracy (see examples in table 8.2). The ranges described in literature for CdTe devices contacted with Au are in the range 0.30 - 0.6 eV [11–18], where the lower values of ϕ_b are seen in

stressed samples, and are thought to be related to Cu diffusion [17]. Some of the values in this work are significantly lower than those reported, and are particularly seen in the Cu containing samples in chapter 7, and are ~0.2 eV lower than the usual values of 0.4 - 0.45 eV. This degree of reduction in barrier height with Cu addition was predicted using SCAPS modelling by Gretener (albeit from a higher predicted as-grown value of $\phi_b = 0.70$ eV) [19]. Consequently, the reduced values seen in this work are thought to be reasonable for the samples in chapter 7, but the low values seen in some Series 522 cells (CdS:O devices with varied Cl treatment) are likely to have a high associated error related to the 'kink' seen in the forward bias curves.

Sample 1	**Cl anneal time** (mins)	ϕ_b (eV)	**Sample 2**	**Cl anneal time** (mins)	ϕ_b (eV)
521/4	20	0.422 ± 0.006	621/3	20	0.430 ± 0.002
521/5	25	0.34 ± 0.08	721/1	25	0.353 ± 0.002
521/6	30	0.391 ± 0.005	622/33	35	0.398 ± 0.002

Table 8.2: Examples of comparison of calculated values of ϕ_b for similar CdS/CdTe chloride treated devices across four different sample sets.

Almost all of the studied devices showed evidence of multi-step tunnelling. There were some notable exceptions, such as the as-grown CdS and CdS:O samples in Series 621, which demonstrated ideal behaviour, and recombination in the depletion region respectively. The dark $J-V-T$ data from two most optimised cells in the chloride treatment time studies, 521/5 and 522/6 (CdS and CdS:O window layers) did not fit with any transport model, so were unable to be categorised. It is unclear whether the chloride optimisation corresponded with a change in mechanism, or if the cells were more unstable than under or over-treated samples and more prone to degradation during temperature cycles.

The charge transport mechanism of multi-step tunnelling provides information about the electrical junction [20]. The temperature dependence of this model implies that neither emission, diffusion or recombination alone described the voltage dependence of the current. In its simplest form, a conduction electron falls into a band-gap state then tunnels to the valence band. Alternatively the electron tunnels into an available band gap state and then falls into the valence band. The electron can also undergo multiple tunnelling and recombination steps between conduction and valence band, the number of which the calculated value R estimates. This process suggests the presence of a large range of traps at the electrical junction with a spectrum of energies. In chapters 5 and 6, the number

of tunnelling steps were reduced more through chloride processing than annealing alone. An effect of chloride treatment therefore appears to be the reduction in the number of tunnelling steps. After chloride treatment, GBs have been found to contain high concentrations of Cl atoms [21], which makes it likely that the energy spectrum of traps which promotes multi-step tunnelling are present in the GBs. This suggests that a significant role of chloride treatment is to passivate the local field at the GBs. It is interesting that the as-grown devices studied in Series 621 had alternative transport mechanisms to multi-step tunnelling, which perhaps is an indication that the GBs are not involved in current transport in the as-grown devices, and only become energetically favourable after the addition of chloride ions, which is consistent with reports of current flowing primarily through grain interiors in as-grown devices [22].

Reducing back contact barrier height

Chloride treatment does not seem to affect ϕ_b except after over-treatment, when the layers start to break down. However, annealing without chloride treatment appears to reduce the values below 0.40 eV, although devices which were chloride treated after annealing in general had $\phi_b > 0.40$ eV. Simulations by Demtsu *et al* suggested barrier heights of <0.50 eV may have little impact on the V_{OC} [13]. While this work is not able to confirm this finding, there have been several examples of devices with similar performance despite differences in $\phi_b \approx 0.10$ eV (e.g. devices 722/1 and 722/3, [CdS/CdTe cells with CuSCN at the back contact] average $\eta \approx 13\%$, $\Delta\phi_b = 0.08$ eV).

Alternatively, Geisthardt *et al* discuss how the energy barrier at the back contact causes valence band bending which limits hole extraction, but a more significant deleterious effect is created though the corresponding conduction band bending, which acts to reduce the turn-on voltage, and therefore the V_{OC} [23]. Despite the better performing devices in this work tending to have higher turn-on voltages, no connection was seen between turn-on voltage and ϕ_b (see for example Series 721 [CdS/CdTe cells with Cu at the back contact] where ϕ_b varies between 0.20 - 0.35 eV with a negligible change in turn-on voltage or V_{OC}).

Changing trap levels

There have been interesting behaviour trends detected though TAS in this work, including the continually changing levels seen in chapter 5, the possible Cu_{Cd} trap signature present in combination treatment cells in chapter 6, and a similar trap evident in all cells contacted with CuSCN in chapter 7 (and only observed in one device doped with copper). The use of corroborative techniques to determine parameters, such as deep level transient spectroscopy (DLTS) or drive level

capacitance profiling (DLCP) would be of great use, while controlling experiment-induced change in device parameters.

One of the effects of chloride treatment was a progressive modification of deep trap levels with treatment time as seen in chapter 5. A peak in performance corresponded to a local minimum in trap energy, capture cross section and density whilst maximising shallow doping. Devices over-treated with chloride subsequently deteriorated in performance. These findings are consistent with reports of trap behaviour in CdTe devices processed with $CdCl_2$ [24, 25]. Continuing from the discussion in chapter 5, two possible explanations for the observed behaviour include the gradual modification of a continuous spectrum of energy levels to create a linear decline in energies until optimisation is reached (possible through grain boundary modification), or a 'hopping' of the trap chemistry from one defect to another. If the latter case is considered, the most likely traps corresponding to the values of E_{nA} for devices in Series 521 (CdS/CdTe with varied chloride annealing times) are shown in the schematic below.

5 minutes	V_{Cd}/Te_i	0.47 eV
	↓	
10 minutes	Te_{Cd}	0.38 eV
	↓	
20 minutes	Te_{Cd}/Cu_{Cd}	0.28 eV
	↓	
25 minutes	V_{Cd}/Cu_{Cd}	0.22 eV
	↓	
30 minutes	Te_{Cd}	0.38 eV
	↓	
40 minutes	Te_{Cd}/Cu_{Cd}	0.30 eV
	↓	
50 minutes	Cl_{Te}	0.42 eV

Whilst the above changing of dominant (detectable by TAS) defect species is not an impossible explanation, it does not appear likely.

For comparison, the equivalent traps for the CdS:O samples from Series 522 annealed at 390 °C are shown below;

15 minutes	Cl_{Te}/Te_i	0.43 eV
	↓	
20 minutes	Te_{Cd}/Cu_{Cd}	0.33 eV
	↓	
25 minutes	Cu_{Cd}	0.31 eV
	↓	
35 minutes	possibly Cu_{Cd}	0.27 eV
	↓	
40 minutes	Cu_{Cd}	0.30 eV
	↓	
60 minutes	Te_{Cd}/Cu_{Cd}	0.32 eV

This progression appears more probable, with a tendency towards the Cu_{Cd} defect in the highest performing devices (perhaps related to the concomitant anneal rather than the presence of chloride), yet there are still considerable chemical defect changes. A more probable explanation was explored in chapter 5 5.4 c), namely that the observed variation in trap energies was a measurement of the grain boundary itself, which was progressively modified with chloride treatment. After saturation of the grain boundaries, it is then speculated that longer chloride duration causes an accumulation of chloride at the CdS/CdTe junction, causing increased resistance and subsequent degradation in performance.

Ultimately it is not possible from these data sets to determine what the measured energy levels are, but expanding the data set with several sample plates for each treatment time, and increasing the number of time data points, should be able to identify a linear vs a stepwise change in energies as a function of chloride treatment time, which would discriminate between a continuous modification of energies and a series of discrete energy levels.

Increasing shallow doping

In chapter 7 it was demonstrated that the addition of Cu ions can improve device performance, despite the observation that uncompensated doping in Series 721 decreased with increasing copper concentration. Trap levels thought to be related to the defect Cu_{Cd} were found in one Series 721 device (CdS/CdTe cells with Cu

at the back contact) and all Series 722 cells (CdS/CdTe with CuSCN at the back contact). This defect is considered to be a dopant, despite its deep nature (usually a single acceptor). This is explained by Perrenoud *et al*, who suggest the low concentration of dopants and the high activation energy ($E_a \gg \mathrm{k}T$) leads to an ionisation degree, ξ_a as follows;

$$\xi_a \approx 1 - \frac{N_A}{N_V}\, exp\left(\frac{E_a}{\mathrm{k}T}\right) \tag{8.1}$$

With low values of N_A, ξ_a approaches 1 (for example, $\xi_a = 94\%$ at 300 K if $N_A = 1 \times 10^{13}\,\mathrm{cm}^{-3}$ and $N_V = 1.8 \times 10^{19}\,\mathrm{cm}^{-3}$) [26].

Theoretical work by Ma *et al* discussed how the local stoichiometry and chemical potential of Cd atoms could influence the carrier concentration. It was suggested that in Cd-rich growth conditions, where the chemical potential of a Cd atom was close to zero, the formation energy of the interstitial defect $\mathrm{Cu_i}^+$ is lower than that of $\mathrm{Cu_{Cd}}$. In this scenario the Cu prefers to migrate to the interstitial sites, which in turn act to compensate p-type dopants. Hence increasing the Cu concentration actually decreases the hole concentration. When the local lattice is Cd poor however, the chemical potential of Cd atoms is increased, and the formation energy of $\mathrm{Cu_{Cd}}$ is lower than $\mathrm{Cu_i}$, such that Cu prefers the substitutional $\mathrm{Cu_{Cd}}$ defect instead. As this site acts as an acceptor through the partial ionisation in equation 8.1, the hole concentration increases [5].

This explanation is now applied to the devices studied here. Following chemical etching, the CdTe is Cd poor at the back contact in order to increase local doping, and therefore improve the Schottky junction. In this region, using the argument above, any Cu present would be more likely to form the acceptor dopant $\mathrm{Cu_{Cd}}$ defect. This would act to increase the local doping further and improve the contact properties. Elsewhere in the device where it is assumed the stoichiometry is no longer Cd rich, the $\mathrm{Cu_i}$ defect would dominate, compensation would increase, and the carrier concentration would drop. This could produce a doping density profile similar to those seen in the Series 721 devices, with an order of magnitude differences between the peak and trough of the 'U' shape doping level across the device. The decreasing acceptor concentration in the bulk (where the chemical potential of Cd would be closer to zero) would decrease with increasing Cu, as was seen in this experiment, while the back contact concentration remained similar, or increased. This explanation would agree with the findings from Series 721.

The improved behaviour of Series 722 (with CuSCN) may be related to local doping. The thiocyanate material is a molecular hole transport material, where the doping is thought to be related to Cu vacancies (and possibly CN vacancies)

[27,28]. The instability of Cu^+, and its tendency towards disproportionation may make it energetically favourable to diffuse into the CdTe from the thiocyanate layer. This diffusion of Cu species to the CdTe bulk is speculated to increase doping of the thiocyanate, as well as increasing the Cu_{Cd} defects in the Cd-poor back surface of the bulk CdTe. This might be capable of producing the more graded doping profile seen in Series 722 devices.

8.3 Factors found to improve V_{OC}

Throughout all the samples studied, a value for V_{bi} has been calculated from $C-V$ analysis. The use of illuminated $J-V-T$ studies in Series 621 demonstrated the consistent values of V_{bi} with treated (thermal and chloride annealed) samples, but not with as-grown sample plates. This increases confidence in the $C-V$ derived results for the annealed or chloride treated devices. As would be expected, $V_{bi} > V_{OC}$ for all tested samples. Despite these values for V_{OC} being somewhat limited by voltage loss across the back contact, they are still significantly lower than the recent single crystal devices, which were reported to demonstrate V_{OC} $> 1\,\mathrm{V}$ [29,30].

Several devices demonstrated higher values of V_{OC} than their peers. Factors which promoted higher voltages are:

CdS:O window layer The 621/6 CdS:O/CdTe chloride treated device had the highest V_{OC} of all studied devices (average $\sim 0.8\,\mathrm{V}$) [31]. This could be related to reduced lattice mismatch between CdTe and CdS:O, and reduced diffusion of Te into the CdS layer minimising the consumption of the CdS layer [32]. (The improvement in V_{OC} has also been elsewhere ascribed to an improved diode activation energy, which describes the relationship of J_0 with T, although this was found not to be the case in the Series 621 devices [33,34]).

Annealing prior to chloride treatment Devices which were annealed prior to chloride treatment have been shown to demonstrate evidence of increased doping and possible Cu_{Cd} levels, possibly though reducing crystal defects and increasing Cu diffusion into the CdTe bulk [19]. Similar improvements in V_{OC} have been reported in devices annealed after $CdCl_2$ treatment [35].

Chloride optimisation Speculated to affect the cell through passivation of the grain boundaries allowing them to become efficient current collectors [36].

CuSCN layer at the back contact Potentially improving the Schottky junction by increasing the local doping, preventing the Cu from diffusing away from the back contact which is associated with cell degradation [37, 38].

It is not clear if the effects of these are cumulative, and if a device processed in a way which included all of these elements would exhibit higher values of V_{OC} still. It is likely that some processes (such as annealing of a CdS:O/CdTe sample at 450 °C prior to chloride treatment) would be incompatible and reduce device performance. However, the areas of impact for these four processes are slightly different, suggesting that (preventable to some degree) voltage losses occur at the front junction, back junction, grain boundaries and within the grains themselves - or rather, in all parts of the cell. As such, the solution to improved V_{OC} in CdTe thin film devices is likely to require the continuation of the multi-factorial approach which has been ongoing for over 30 years, with advancements in each of these areas separately (whilst not diminishing improvements made elsewhere), rather than a simple solution.

8.4 Implications for improving cell performance

The preceding chapters have provided evidence which supports the use of $MgCl_2$ as an alternative agent to $CdCl_2$ for activation of CdTe thin film solar cells. Although no improvements in cell efficiency have been demonstrated with $MgCl_2$, the non-toxicity and cheap price of this compound has the potential to significantly reduce the manufacturing costs of CdTe modules. This in turn could promote the position of CdTe thin film technology in the photovoltaic market.

Other manufacturing techniques have been explored which have been shown to improve cell performance, namely a thermal anneal prior to chloride processing, the use of a CdS:O window layer, and the deposition of a CuSCN layer under the back contact. It is possible these techniques could be used singly, or perhaps in combination, to improve module efficiency.

8.5 References

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9. Conclusions and further work

9.1 Conclusions

This thesis presented a series of experimental investigations of the influence of processing and device structure on the underlying electrical features of CdTe thin film solar PV devices.

- Structures and processing explored:
  - The use of $MgCl_2$ instead of the more widely used $CdCl_2$ to process CdTe solar cells.
  - The time dependence of the effects of chloride treatment on both the performance of devices and the underlying electrical behaviours.
  - The separation of the effects of thermal annealing alone to annealing with chlorides.
  - The effects of window layers (both CdS and CdS:O) on underlying electrical behaviour.
  - The effects of back contact doping on the deep and shallow trap levels.
- Methods used were as below:
  - $J-V-T$ studies were used to investigate transport phenomena and back contact behaviour.
  - Shallow doping profiles were determined through $C-V$ analysis.
  - Thermal admittance spectroscopy was used to study deep trap behaviour.
  - Device electrical structure was investigated through equivalent circuit analysis.

In chapter 5 the developments of electrical parameters with processing time was evaluated in detail for $MgCl_2$ cells with both CdS and CdS:O window layers. It was found that:

(a) There was a shallow peak in efficiency with $MgCl_2$ processing time.

(b) There was a much sharper coincident peak in shallow doping.

(c) The deep level behaviour was complex:

  (i) The energy levels changed as a function of processing time.

  (ii) The deep energy levels were lowest values in the most efficient devices. This is consistent with what is expected in Shockley-Read-Hall recombination.

(d) High performance was associated with reduced series resistance.

The deep trap evolution could in principle be explained by a) a continuously varying energy level as had been postulated by Lourenço for grain boundary related traps [1], or b) the switching through a series of energetically separate trap levels as the exposure to chloride progressed. Of the two explanations b) appears unlikely, not least due to the significant changes in defect chemistry that it would require. Indeed the evidence supports the continuously varying trap model, although further data points would be required to verify this conclusively.

The aim of chapter 6 was to test the hypothesis that simple thermal annealing and annealing in the presence of $MgCl_2$ had separate effects on the device performance and underlying behaviours. Cells having window layers of CdS and CdS:O were tested. It was found that:

(a) CdS:O cells had higher V_{OC} and η than CdS, with reduced series resistance.

(b) Thermal annealing increased J_{SC} and shallow doping levels.

(c) $MgCl_2$ treatment increased V_{OC} and R_{SH} while reducing R_S compared to thermal annealing alone.

(d) Thermal annealing prior to chloride processing boosted V_{OC}, FF, acceptor density, and η.

Annealing prior to chloride treatment may have the action of improving performance, possibly through increasing the shallow doping concentration. There appears to be an inverse relationship between temperature and anneal duration, such that cooler temperatures require longer anneal durations to provide the same performance benefit. It is possible the effect could be replicated by conducting a

very short (seconds or minutes) anneal at a high temperature (a rapid thermal anneal), but further studies would be required to explore this relationship further.

In chapter 7 the influence of changing the doping at the back contact was examined using copper and copper thiocyanate. It was found that:

(a) The improved η of copper-doped devices did not correspond with a higher level of shallow doping in the active region.

(b) Copper thiocyanate devices had higher V_{OC} and η than those doped with copper alone.

(c) The Shottky barrier height at the back contact decreased with increased copper doping.

(d) A higher level of shallow doping was consistently seen in the copper thiocyanate contacted cells.

It is speculated the increased performance and higher level doping profile in the copper thiocyanate devices may indicate that the CuSCN may control diffusion of Cu into the device bulk, therefore maintain higher doping at the back contact and improve the Schottky contact.

Overall, the studies of CdTe treated with $MgCl_2$ have produced results which have been consistent with literature reports for $CdCl_2$ processed devices. This implies that any deleterious effects from addition of magnesium to the layer are negligible compared with the benefit that the chloride provides. However, there was no evidence in this work that the performance with $MgCl_2$ could exceed that from $CdCl_2$. This being said, the material's low cost and lack of toxicity has the potential to reduce the \$/Wp price of CdTe modules.

9.2 Suggestions for future work

i. Further sample data points for the studies in chapter 5 would be desirable to determine the mechanism of trap energy evolution. Corroboration of the deep trap observations with a technique such as DLTS could prove enlightening.

ii. The finding that pre-annealing (thermal only) prior to $MgCl_2$ annealing has increased PV performance was encouraging, but in this work the device efficiencies were $\sim$8%. This study would be worth repeating with higher efficiency devices for which factors other than the contact may extend the efficiency. An extension to the range of processing conditions explored would be informative, including for example rapid thermal annealing.

iii. The encouraging results from the use of copper thiocynanate would suggest that further device optimisation with this compound would be worthwhile in order to achieve high efficiency devices.

iv. To investigate effects from addition of magnesium to the device, a study of deep and shallow traps in $MgCl_2$ treated CdTe devices with a thin layer ($\sim$nm) of Mg applied before Au contacts may expose defects which have been too low in concentration to be detectable by the methods used in this thesis.

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APPENDIX

Appendix A Thermal Admittance Spectroscopy: Worked Example

This appendix demonstrates the application of the Thermal Admittance Spectroscopy (TAS) methodology as described in section 4.3.4.2 (apparatus) and 3.3.3 (theory). The sample was are chosen to exemplify the usual trends and challenges with the technique. It is sample 622/19, a CdS/CdTe solar cell air annealed at 500 °C for 60 min before $MgCl_2$ processing.

The experimental apparatus, measurement conditions and general procedures are described in section 4.3.4.2. For the experiments described in this work, all admittance spectroscopy was conducted by taking capacitance and admittance data over a core temperature range of 110-310 K. Experiments which were conducted at lower (70 K) or higher (320 K) temperatures had previously been found to permanently alter the cell response, i.e. the process of measuring the samples was damaging the samples. The restricted temperature range was therefore chosen to improve reproducibility and allow further experiments.

A typical example of the raw capacitance (C) and conductance (G) data at zero bias as a function of frequency (f) for the stated temperature range is seen in figures A.1 a) and b) respectively. From A.1 a) it can be seen that the low temperature capacitance value of ~1.5 nF does not vary significantly from low to high frequency. At low temperatures the carriers have been frozen out and the material is acting as a dielectric, with the value of the capacitance equal to the high frequency value, which itself is equal to the geometrical capacitance, $C_g = \frac{\varepsilon A}{t}$ where A is the area, and t the thickness of the film [1]. As the temperature is increased, the low frequency capacitance starts to increase, up to a value > 3.5 nF at 300 K. The frequency at which the capacitance changes from its low frequency value to the geometrical capacitance is dependent on the temperature. Traps can affect this temperature dispersion. A similar dispersion can be seen in the conductance data in figure A.1 b) and the inset shows the behaviour for 230 K as a typical example. At low frequencies the traps can respond to the test signal,

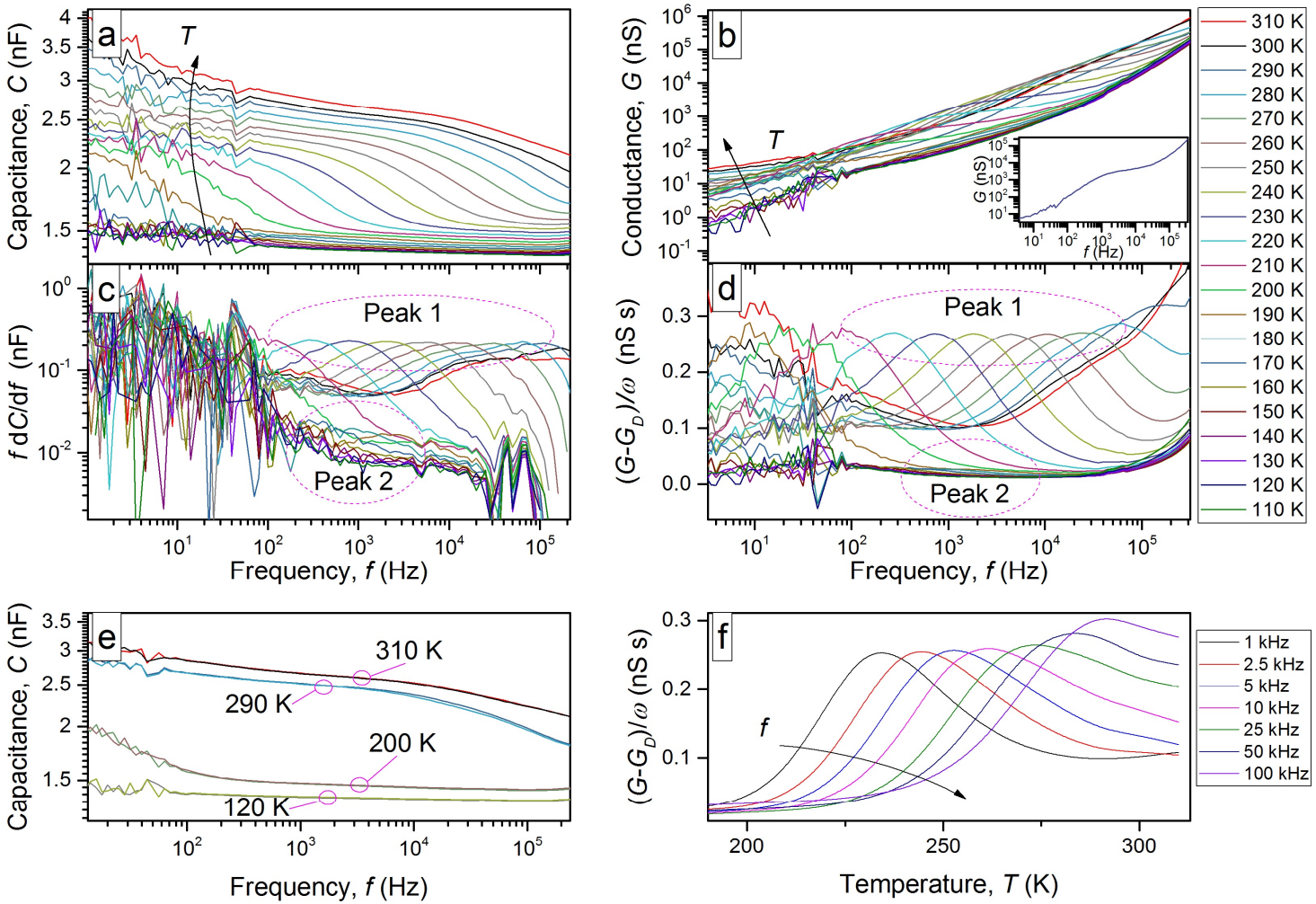

Figure A.1: Typical TAS data using sample 622/19. Plots show raw a) capacitance and b) conductance data. This data is then manipulated to aid location of the frequency response step change, using c) the differential capacitance $-fdC/df$ and d) reduced conductance $(G - G_D)/\omega$ [where G_D is the DC value of conductance). Plot e) shows examples of the pairs of temperature dependent C - f data taken with both increasing and decreasing temperature sweeps (see text). In f) the reduced conductance peak can be seen to move towards higher temperature with higher frequencies.

but at higher frequencies the emission rate, e_n, of the traps is too slow for them to contribute. The frequency at which this change occurs is related to e_n at the measurement temperature, and the trap density N_t can be calculated from the magnitude of the change [2].

In order to accurately find the frequencies at which the step change occurs, the capacitance and conductance data are analysed slightly differently: The differential of the capacitance, $-fdC/df$, is calculated as seen in A.1 c), where the peaks correspond to the position of the step change, whereas for the conductance the 'reduced conductance', $(G - G_D)/\omega$ is used in a similar way as seen in figure A.1 d) [G_D is the DC value of the conductance, in practice this being for 1 Hz]. In both plots it is possible to see two clusters of peaks which move with temperature. The cluster labelled 'Peak 1' is first apparent towards room temperature at high frequencies, and shifts to lower frequencies with reducing temperature. The second cluster, 'Peak 2', is much smaller in magnitude as a consequence of the lower trap density. The peak frequencies are identified from Gaussian fits. These values are then used to populate the Arrhenius plot as seen in figure A.2 a).

Two checks are conducted on the data to ensure reliability. As described in section 4.3.4.2 the electrical measurements are taken twice for each sample at each temperature, once with the temperature reducing stepwise (temperatures 290 K to 110 K), then repeated as the temperature is increased (110 K to 310 K) before returning to room temperature (310 K to 290 K). The plot in figure A.1 e) shows pairs of temperature data across this range. The vales for the sample shown are virtually identical, with only a slight change in the step position for the first and last readings taken (290 K). For such samples the data was combined before analysis. Occasionally samples would demonstrate a more significant change between the first and second readings. For these only the first temperature readings were used for analysis. A second check routinely performed on the data was to monitor the positions of the reduced conductance peaks as seen in figure A.1 f). A peak which increases in temperature as the frequency is increased is a distinctive feature of thermionic emission, suggesting that it is amenable to analysis using an Arrhenius plot in the usual way [2, 3].

Following the creation of an Arrhenius plot as seen in figure A.2 a) a straight line fit to the data will allow calculation of the thermal emission pre-factor, ξ_0, and activation energy, E_A, from the intercept and slope respectively using equation 3.16 [4]. If the correct value of ξ_0 has been determined, trap density plots calculated from the capacitance using equation 3.18 will superimpose, with a peak evident at the same energy value as the E_A determined from the slope of the Arrhenius plot.

This can be seen for two separate trap signatures in figures A.2 b) and c).

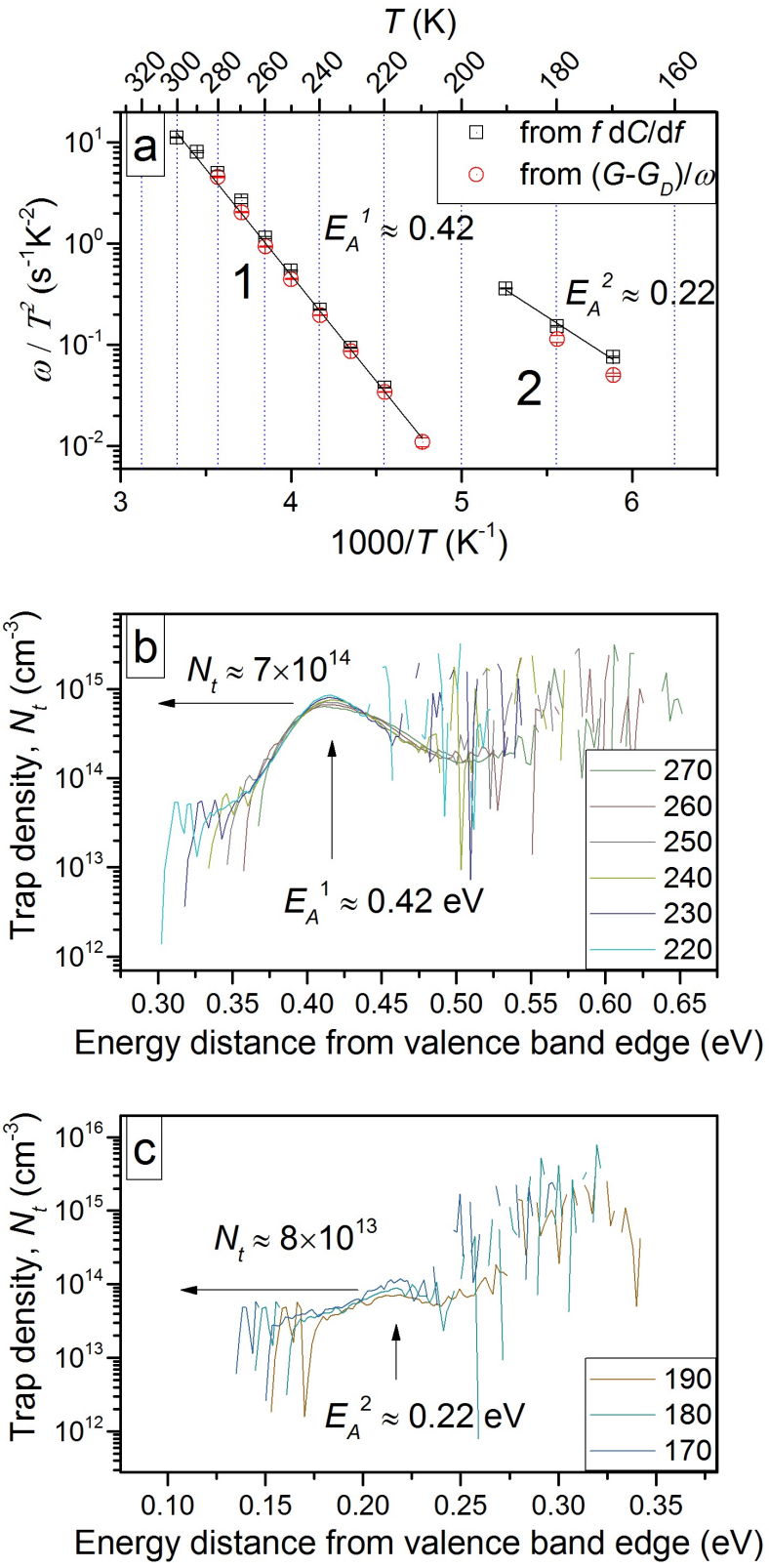

Figure A.2: Graphs of frequency response data for cell 622/19 showing a) the Arrhenius plot [where ω uses the peak positions from plots A.1 c) and d)], b) the plot of equations 3.14 and 3.18 [using the intercept value from the linear fit 1 from a) to calculate ξ_1] showing overlapping energy plots with the peak at the value of the Arrhenius gradient, c) a similar plot with ξ_2 calculated from the intercept of linear fit 2 from a).

The x-axis of these plots is an energy scale using the determined value for ξ_0 (see equation 3.18). The y-axis values are scaled by the calculated value of V_{bi} from $C-V$ analysis (see chapter 3.3.2). In figure A.2 b) there is a single distinct peak centred at 0.42 eV. As is typical for these plots, where the peak is evident the data is smooth and continuous. (Elsewhere the data is noisy, and the use of log terms in the analysis (see equation 3.14) leaves gaps in the data where the lines are broken. The use of a semi-log axis to present the data leaves additional gaps in the data.) For this trap signature the peak is located at the value for E_A^1 extracted from the Arrhenius plot, acting as confirmation of an appropriate value for ξ_0^1. In figure A.2 c) there is a weaker peak visible, which is consistent with the lower trap density, an order of magnitude smaller that for figure b). Despite the smaller signal, the overlap at the value of E_A^2 extracted from the linear fit 2 from A.2 a), combined with the presence of peaks in both the differential capacitance and reduced conductance plots as seen in figure A.1 c) and d) [labelled 'Peak 2'] increases confidence that this is a genuine trap signature. The physical energy separation from peak 1, and the presence of the peak cluster in the mid frequency range, gives confidence that this signature is not a misleading back-contact-induced artefactual high-frequency tail from peak 1 [5].

For some samples, despite a clear peak being evident on the energy plot, the presence of a small number of data points on the Arrhenius plot made an accurate assessment of ξ_0 and E_A difficult. In this situation a Gaussian was fitted to the energy peaks for a variety of values of ξ_0, and the changing distribution of values for E_A allowed for selection of the value for ξ_0 for which the standard deviation in E_A was the smallest.

For the sample studied in this worked example the following parameters have now been determined:

	Trap 1	**Trap 2**
E_A Arrhenius [eV]	0.417 ± 0.001	0.217 ± 0.004
E_A N_t vs E [eeV]	~0.42	~0.22
N_t [cm^{-3}]	$\sim 7 \times 10^{-14}$	$\sim 8 \times 10^{-13}$
σ_p [cm^{-2}]	$(4.7 \pm 1.3) \times 10^{-17}$	$(2.95 \pm 0.13) \times 10^{-14}$

Table A.1: The results from analysing the TAS signal of sample 622/19, producing values for E_A, N_t and σ_p for two energy levels.

A.1 References

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Appendix B Methods of extracting parameters from $J-V$ curves

$J-V$ curves can be used to estimate device parameters such as series resistance, R_S, and diode factor n. There are numerous models which can be applied to the data, each returning different results. The most appropriate models for CdTe cells are shown in the equations below, and are useful for: devices dominated by multi-step tunnelling (equation 2.12), a model described by Sah, Noyce and Shockley (equation 2.8) [1], or devices which can be described using a single diode model (equation 3.4). Fitting the last of these three equations can be time consuming and problematic, as J appears on both sides of the equation, and iterative methods are required to determine parameter vales. As there are five free parameters in this intrinsic equation, good initial parameter estimates are required to produce a good fit.

Multi-step tunnelling equation

$$J_f = J_0\, exp(AV) \tag{2.12}$$

Sah, Noyce and Shockley equation

$$J = J_0\left(exp\left[\frac{\mathrm{q}V}{n\mathrm{k}T}\right] - 1\right) \tag{2.8}$$

Approximation

$$J \approx J_0\left(exp\left[\frac{\mathrm{q}V}{n\mathrm{k}T}\right]\right) \tag{B.1}$$

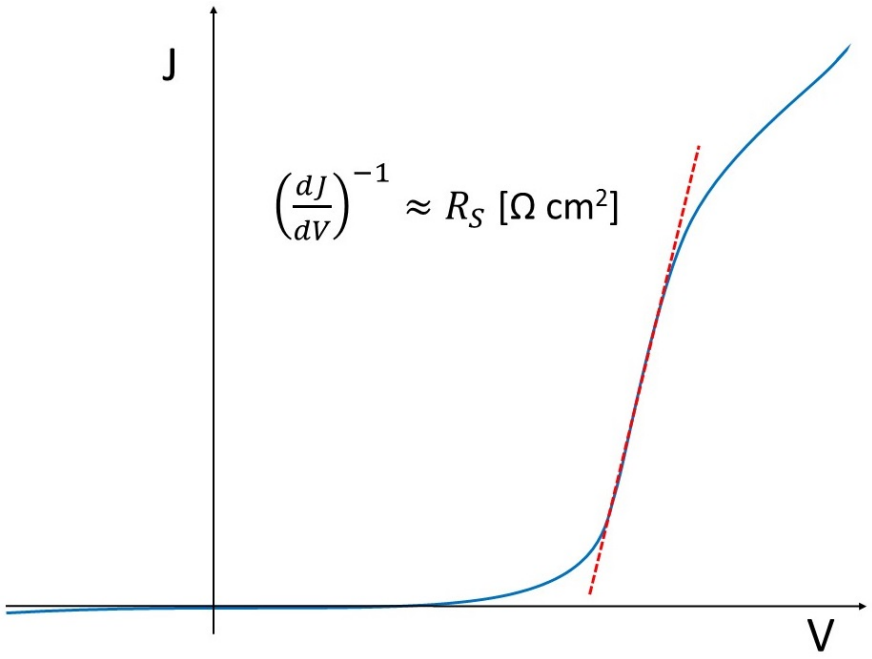

Figure B.1: A schematic of how to extract the R_S from a dark $J-V$ curve.

Single Diode equation

$$J = J_0\left(exp\left[\frac{V-(JR_s)}{n\mathrm{k}T}\right]-1\right)+\frac{V-(JR_s)}{R_{sh}} \tag{3.4}$$

An alternative method to calculate R_S is celled the 'Slope' method, and is described below.

Slope method

The series resistance affects the $J-V$ curve in forward bias, and can be estimated from the slope as shown in figure B.1 [2]. This is an estimate only, and for CdTe cells unlikely to be sufficiently accurate to analyse light $J-V$ data [3]. However it is still sufficiently accurate to have been used in several studies [4–6]

It is possible to fit equation 2.8 to $J-V-T$ data. An example for Series 521 can be seen in figure B.3. It is possible to simplify equation 2.8 to equation B.1 without significant loss of accuracy.

For Series 521, the diode factor n was calculated both through estimation via the slope method, (where the gradient, A of the lnJ vs V graph derives from the equation B.2 below, and through modelling with the Sah, Noyce and Shockley equation).

$$lnJ \approx ln\, J_0 + \left(\frac{\mathrm{q}V}{n\mathrm{k}T}\right) = lnJ_0 + AV \tag{B.2}$$

where

$$A = \frac{\mathrm{q}V}{n\mathrm{k}T} \tag{B.3}$$

A comparison of the values obtained for n for this Series is shown below. As has been discussed in chapter 5.3.1.2, although the value n has no physical relevance in multistep processes, it can nevertheless be a useful tool used to identify common transport mechanisms. For this series, and for the other series used in this work, it was found that the slope method produced a value of n that was in good agreement with the Sah, Noyce and Shockley equation (equation 2.8) at room temperature. However, towards 200 K the results diverged, with the slope method consistently resulting in a higher value. However the trends of n with T were identical for both methods. The fit of equation 2.8 is generally superior to the multistep approximation. However it can be difficult to obtain good quality fits towards cooler temperatures, whereas the slope method is almost always possible. Therefore, when discussing the trends of n with T the slope method value of n is used, but for the room temperature value of n, that of the Sah, Noyce and Shockley equation is reported.

In figure B.2 the single diode fits to $J-V-T$ data for sample 521/5 can be seen. Fitting was done using a semi-log J vs V curve in order to aid observation of fit quality. The single diode equation was fitted to the near-linear area of the graph in the voltage range 0.2-0.6 V where the exponential component of the fitting equation was most influential. To obtain initial fits for this implicit function initially all parameters were free, with no initial estimates and large constraints. In cases where the fit provided parameter values that were improbable, the fits were recalculated using different initial estimates. The process for this was as follow; a) a good fit for the 300 K plot was determined through trial and error and careful selection of the voltage range (for which the R_S, R_{SH}, and back contact effects were least influential), b) the parameter values of J_0, n, R_S and R_{SH} for this fit were then used as the initial estimates for the adjacent (lower T) data plot, c) the voltage range of the fit for this adjacent plot was then adjusted to again select the appropriate part of the plot.

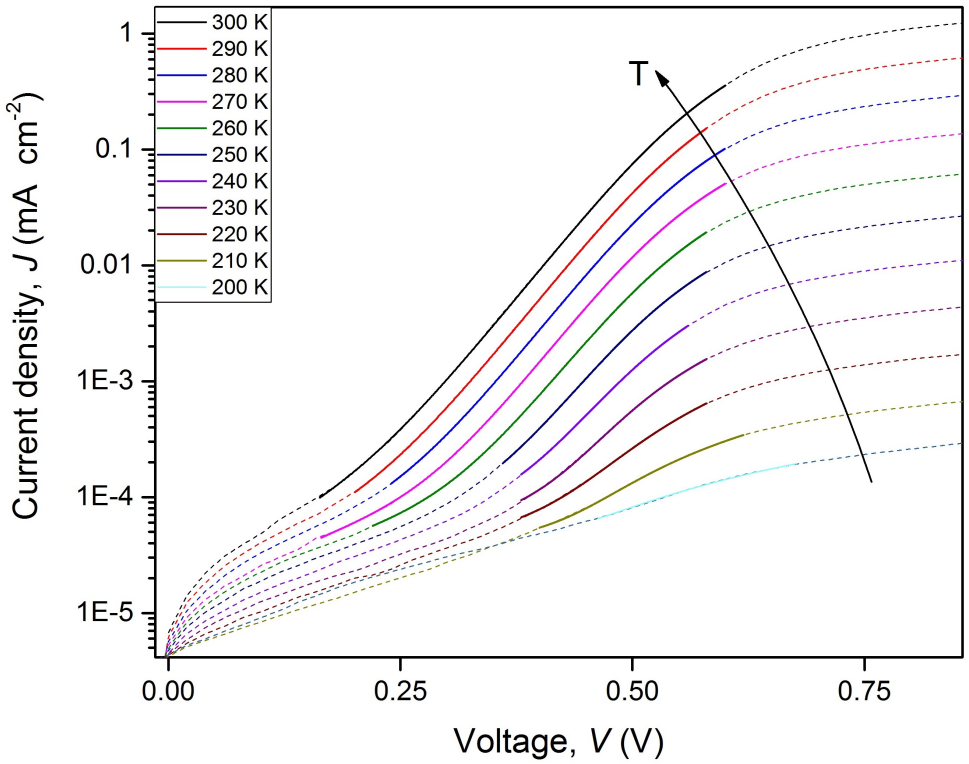

Figure B.2: A graph to show the $J-V-T$ data for sample 521/4 (20 mins) as dotted lines, with the fits to the single diode equation 2.8 as solid lines.

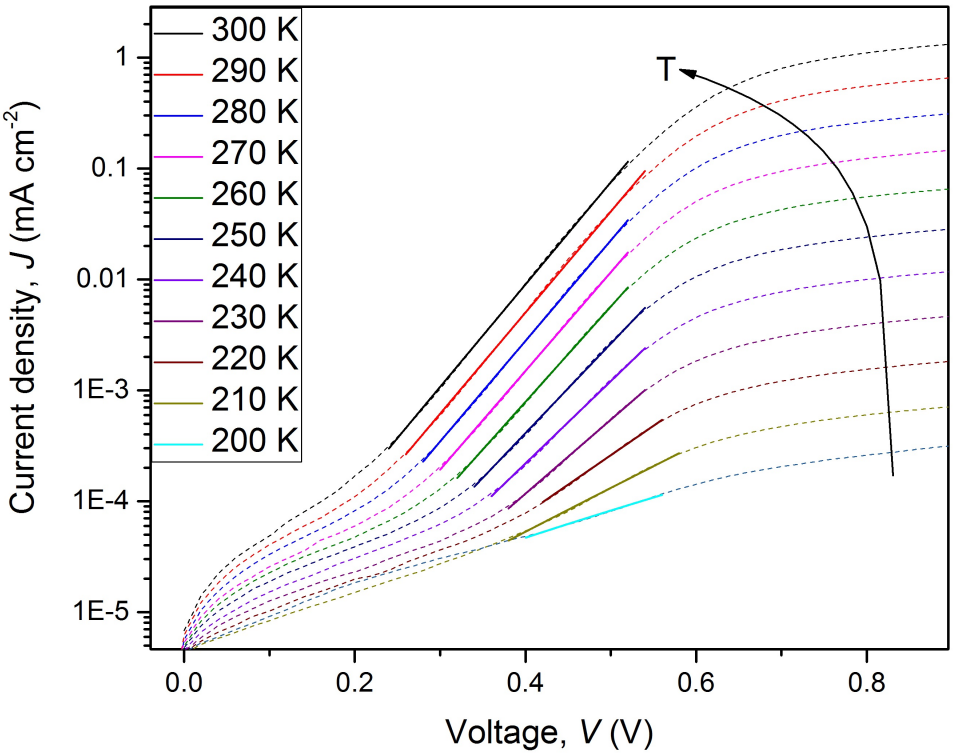

Figure B.3: A graph to show the $J-V-T$ data for sample 521/4 fitted with equation 2.8 to calculate n: the fits (solid lines) are to the data (dotted lines) in the voltage region where the log current graph is linear.

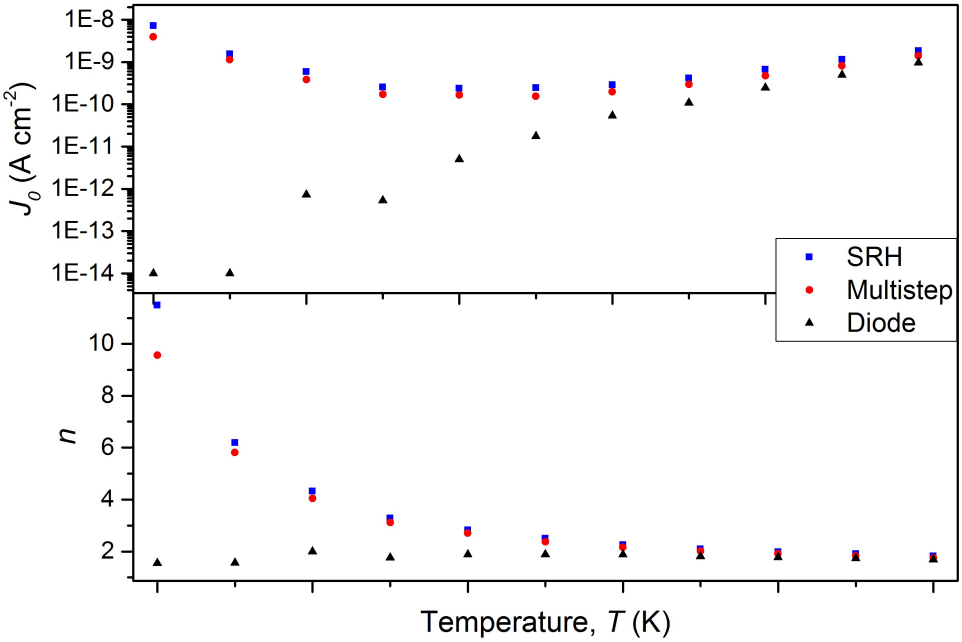

Figure B.4: This plot compares the values of parameters J_0 and n as calculated for sample 521/4, using either equation 2.8 (Sah, Noyce and Shockley), equation B.2 ('Multistep') or equation 3.4 ('Diode')

B.1 References

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Appendix C Interpreting the Mott-Schottky plot

A capacitance-voltage curve in the form C^{-2} vs V (a Mott-Schottky plot) yields information about charge carriers in junction devices. The theory is discussed in section 3.3.2. Performing this analysis on silicon-based technologies is thought to provide accurate results, but unfortunately the situation with many thin film solar cells is more complicated. Significant factors are the importance of light-generated carriers in CdTe cells which are in part responsible for the crossover between light and dark $J-V$ curves, and also light-related trapping of photo-generated charges which increases the capacitance of the junction. Illuminated $C-V$ curves in CdTe differ from dark curves as a consequence. In practice, light or dark $C-V$ curves rarely adopt the text-book linear shape from which free carrier doping and built-in voltage can be ascertained. Certainly all the samples examined in this work have more complex behaviour (see illuminated and dark CV measurements at 300 K data in section 6.2.2).

C.1 Theory

As discussed in section 2.1.2 the V_{bi} is related to the V_{OC} through the following equation [1].

$$V_{OC} = V_{bi} - \frac{A\mathrm{k}T}{\mathrm{q}} ln\left(\frac{\mathrm{q}pv_r}{J_L}\right) \tag{2.1}$$

where V_{bi} is the built-in voltage, A is the ideality factor, k is the Boltzmann constant, T is the temperature, q is the electron charge, p is the hole density, v_r is the recombination velocity and J_L is the photocurrent.

The V_{OC} for inorganic solar cells appears to be limited by the V_{bi} (although this is not necessarily true for organic devices [2]). However it is entirely possible to extract a value for $V_{bi} < V_{OC}$ from a Mott-Schottky plot, depending on the voltage range used. For the calculations in this work the V_{bi} was calculated from the x-

axis intercept of a Mott-Schottky line fit, where the intercept is $(V_{bi} - V_D)$ [3]. V_D is the band bending due to the Fermi level. However this does assume uniformly doped material and an abrupt $p-n$ junction. This correction to the V_{bi} is related to the band bending of the Fermi level, E_F, which in silicon is of the order of kT. In other materials it can be significantly larger, having values in CdTe from 0.1-0.8 eV [4]. Without correcting for this, many values of V_{bi} are *less* than V_{OC}, which is unphysical. In order to provide a more accurate value for V_{bi}, the band bending related to the local Fermi level is calculated as follows:

$$V_D = \frac{\mathrm{k}T}{\mathrm{q}} ln\left(\frac{N_A}{N_V}\right) \tag{C.1}$$

where a value of $4.5 \times 10^{19}\,\mathrm{cm}^{-3}$ is assumed for the density of states in the valence band, N_V [5], and the value of N_A is estimated from the Mott-Schottky plot.

C.2 Data

In order to decide upon a protocol for estimating the doping from these plots, attempts have been made to extract the parameters N_{nA} and V_{bi} from three different voltage ranges across the Mott-Schottky plot; a) low reverse bias, b) neutral bias, around $V = 0$, and c) low forward bias, well below interference from the back contact. These are shown on the plot in figure C.1.

From the plot in figure C.1 it is possible to see that the reverse bias (up to -1 V) curve is almost linear, but has not saturated, indicating the cell is not fully depleted. At 0 V the plot is starting to curve, and it briefly becomes linear at low forward voltage (0.2 - 0.4 V). At voltages higher than ~0.5 V the back contact begins to affect the capacitance and the data becomes unreliable.

The extracted values for V_{bi} for the three different voltage ranges are shown in figure C.2. The reverse bias analysis yields some unphysically high built-in voltages, whereas the neutral range (around $V = 0$) produces far more credible numbers closer to the recognised band gap (~1.5 V). Analysis in the forward bias produces smaller values of V_{bi}, all $V_{OC} < V_{bi} < 1$ V. These correlate well with the extracted data from illuminated $C-V$ analysis in section 6.2.2.

The determined values for V_{bi} from analysis in the forward bias (in the range 0.2 - 0.4 V) are thought to be significantly lower than the actual V_{bi}, as the observed V_{OC} in these samples is 0.6-0.8 V. Even though it is possible to obtain a more (apparently) realistic V_{bi} from the Mott-Schottky plot though analysis over the neutral-bias region, it is thought this approach overestimates N_{nA}, rendering

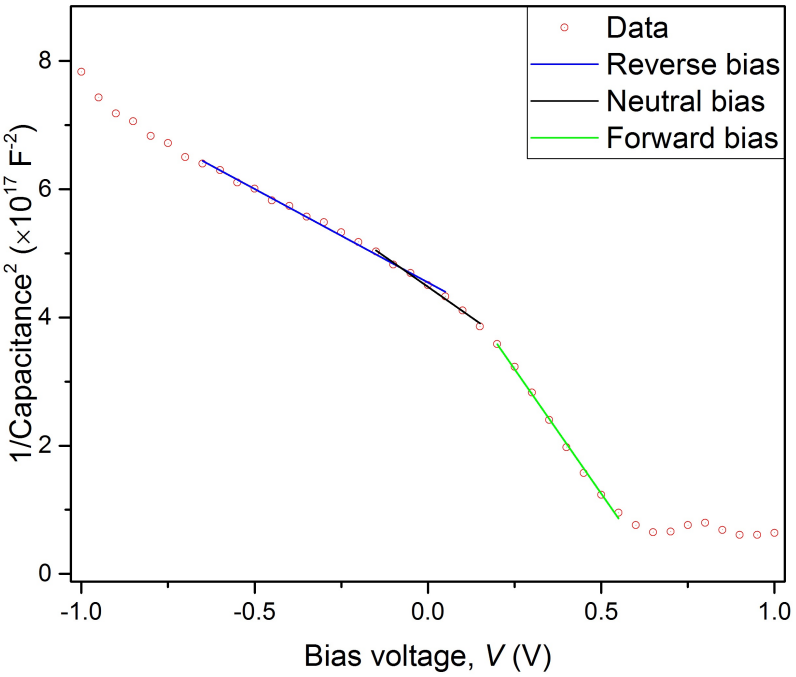

Figure C.1: A Mott-Schottky plot for a CdTe cell in the dark, showing three regions for analysis; low reverse bias, neutral bias (around 0 V), and low forward bias. At high forward bias the capacitance is affected by the expanding junction of the back contact, and is therefore unreliable.

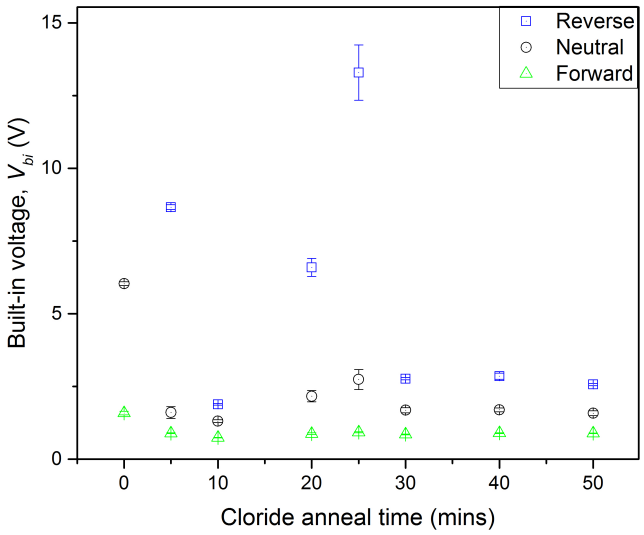

Figure C.2: The extracted values of V_{bi} for Series 521 from the a) reverse bias, b) neutral bias and c) forward bias regions of the plot in figure C.1. Much of the data taken at reverse or neutral bias is unphysical.

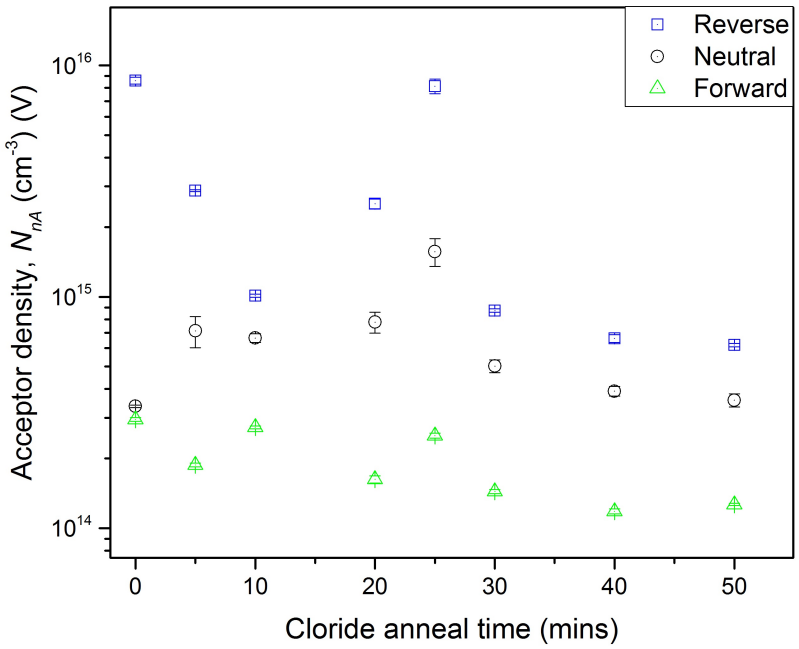

Figure C.3: A comparison of the apparent acceptor density, N_{nA}, for series 521, as determined through analysis of different voltage regions of the Mott-Schottky plot. It can be seen here that although there is an order of magnitude difference between the reverse and forward bias values, all three analysis regimes demonstrate a local peak in acceptor density at 25 mins.

analysis of this part of the plot inappropriate. For a p-type semiconductor the reverse bias linear part of the plot stems from accumulation of charge at either side of the space charge region (SCR), creating high capacitance values and upward band bending. As a forward bias is applied holes are repelled from CdTe bulk towards the CdS layer, and at some voltage a flat-band energy is reached. At this point the carrier concentration is directly related to the bias voltage. In high forward bias an MOS device would display inversion, where the minority carriers become the majority at the $p-n$ interface, leading to downwards band bending - the opposite direction to that in reverse bias. This may also occur in CdTe at grain boundaries. Jiang *et al* [6] found evidence of higher than expected potential at grain boundaries, indicating either depletion or inversion. In either accumulation or inversion, the carrier concentration cannot be estimated accurately, as the free carrier concentration depends exponentially on band bending: only the flat band region of voltage bias should be used, and even this is unreliable if deep traps are contributing to the capacitance to a non-negligible degree [7]. This 'flat band' region corresponds to the linear section of the plot in figure C.1, in this case located in the forward bias, and it is here that the number of free carriers is the best able to be isolated. The narrow width of this voltage region in forward bias is also related to the thickness of a thin film cell, which leads to a strong interactions and intermixing between layers [8].

Following consideration of the above information, the analysis for this work was conducted on the linear section of the Mott-Schottky at low forward bias. While this is expected to produce a systematic error in V_{bi} for all samples through the assumption of N_V, this error is likely to be similar for all samples.

C.3 References

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Appendix D Solar area calculations

The following calculation was used to estimate the amount of area required to produce the world's yearly requirement through solar energy in a short time period.

Assumptions:

i. Solar module efficiency 18%

ii. Constant insolation at AM1.5 producing power density of $1000\,\mathrm{W\,m^{-2}}$

iii. Ideal cell orientation to sun

iv. Demand is 629 Btu [1]

v. Area of USA = 9,826,675 $\mathrm{km^2}$ [2]

Power per unit area:

$$\begin{aligned} 0.18 \times 1000\,\frac{\mathrm{W}}{\mathrm{m^2}} &= 180\,\frac{\mathrm{W}}{\mathrm{m^2}} \\ &= 1.8 \times 10^8\,\frac{\mathrm{W}}{\mathrm{km^2}} \end{aligned}$$

Convert to Wh:

$$1.8 \times 10^8\,\frac{\mathrm{W}}{\mathrm{km^2}} \times 3600\,\mathrm{s} = 6.48 \times 10^{11}\,\frac{\mathrm{W\,h}}{\mathrm{km^2}}$$

Convert demand to Wh:

$$629 \times 10^{15}\,\mathrm{Btu} \times 0.293929 = 1.84 \times 10^{17}\,\mathrm{W\,h}$$

Find area of modules needed to meet demand [$\mathrm{km^2}$]:

$$\frac{1.8 \times 10^{17}\,\mathrm{W\,h}}{6.48 \times 10^{11}\,\frac{\mathrm{W\,h}}{\mathrm{km^2}}} = 283,950\,\mathrm{km^2}$$

Find time to produce demand if area the size of USA was covered:

$$\frac{283,950\,\text{km}^2}{9,826,675\,\text{km}^2} \times 60\,\text{mins} = 1.73\,\text{mins}$$

D.1 References

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